Telemetría de bajo consumo para adquisición remota de datos fisiológicos

Juan F. Döppler

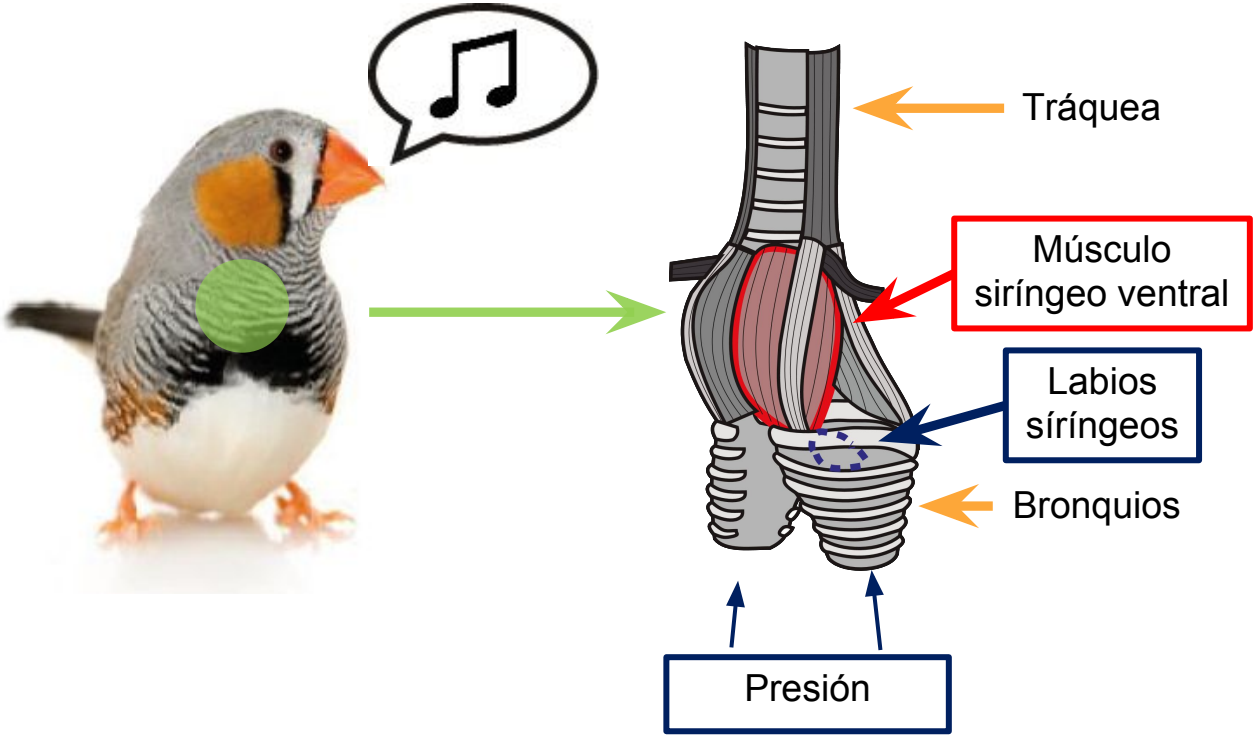
Laboratorio de Sistemas Dinámicos, Departamento de Física, FCEN, UBA

Un poco de contexto: aves oscinas como modelo animal

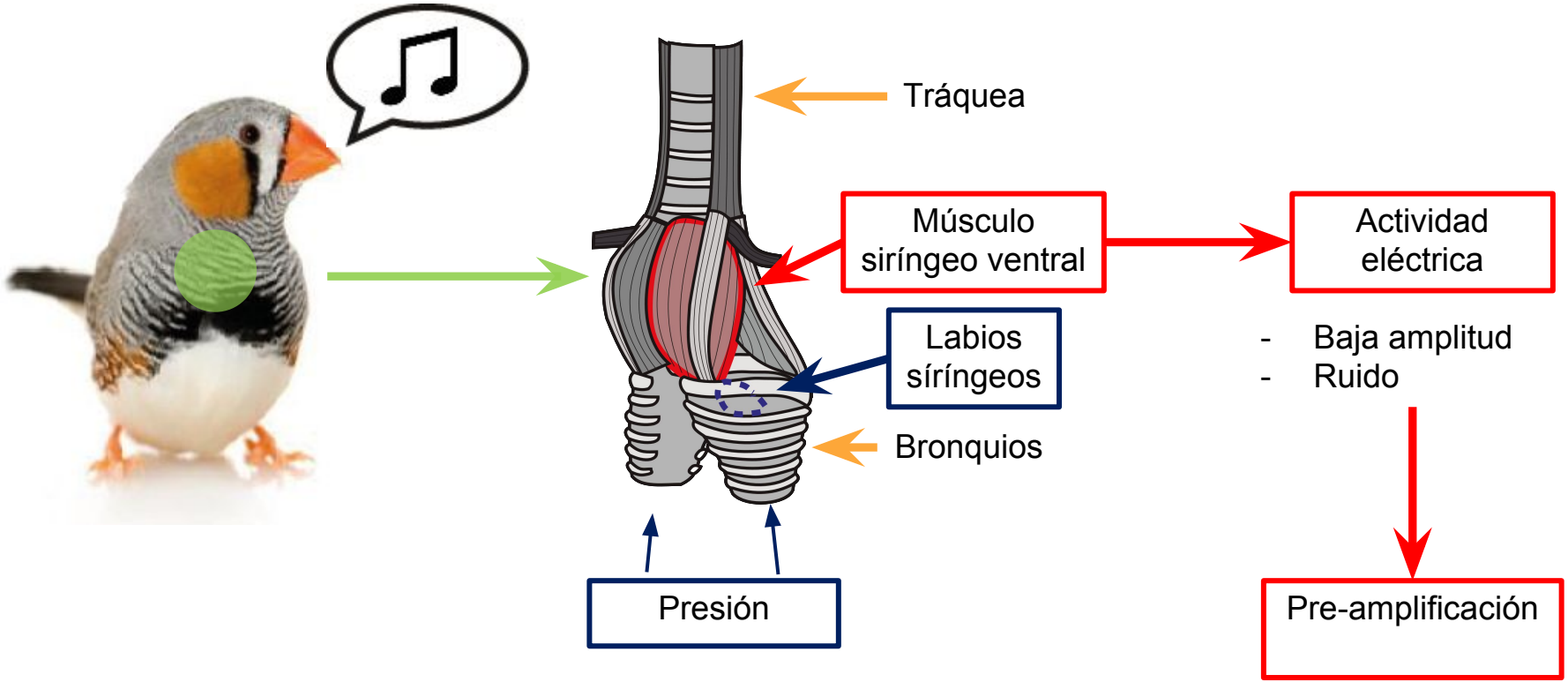
- Etapas de aprendizaje análogas a humanos
- Mecanismos de producción similares
- Especies campeonas para estudio de mecanismos de aprendizaje y producción vocal

Un ejemplo de medición: electromiografía

Un ejemplo de medición: electromiografía

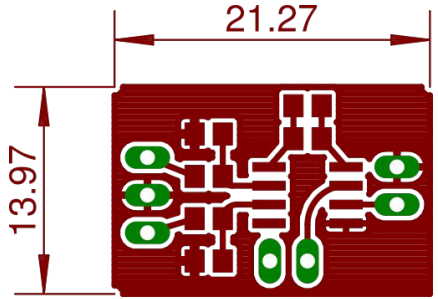


Un ejemplo de medición: electromiografía



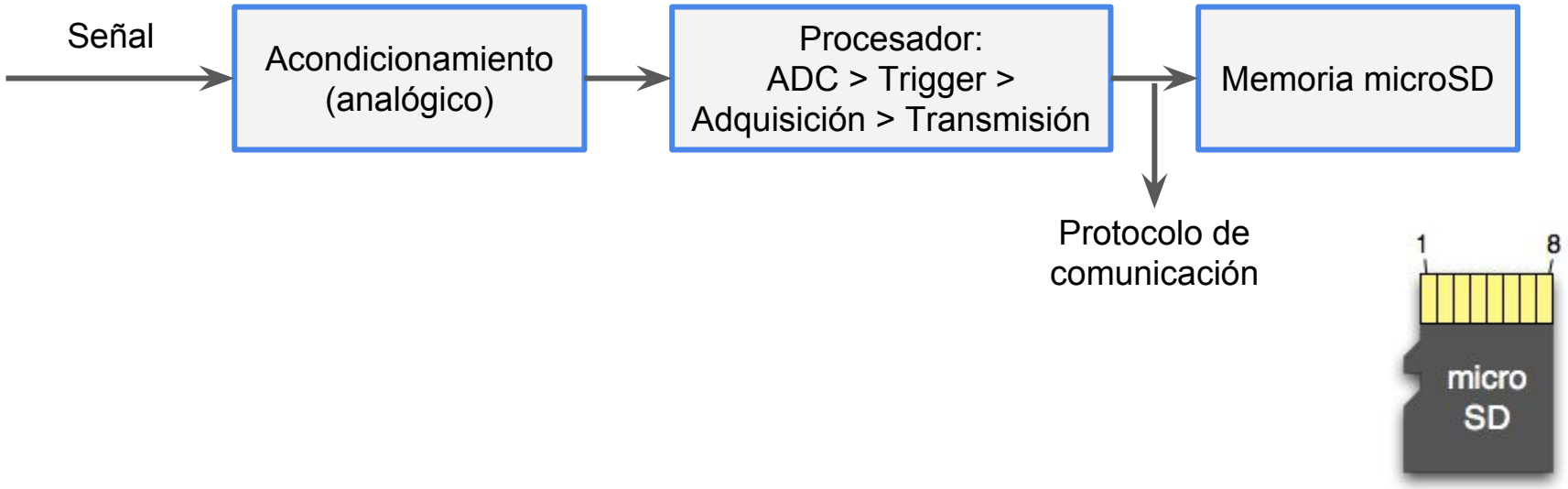
El desafío: mediciones con animales libres

- Tamaño: debe ser portable (~1cm x 2cm)
- Peso: debe ser portable (debajo de 20% del peso)

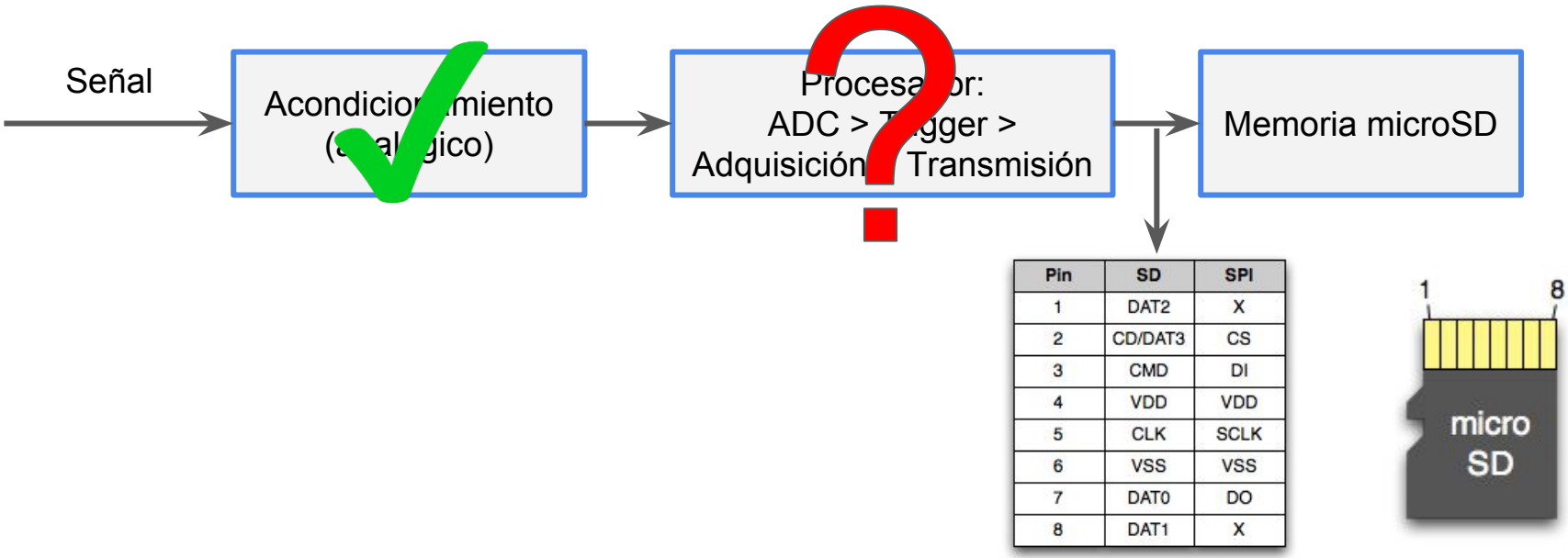


- Bajo consumo
- Autonomía (adquisición)

Propuesta: adquisición remota en microSD usando microprocesador



Propuesta: adquisición remota en microSD usando microprocesador



Microprocesadores MSP430

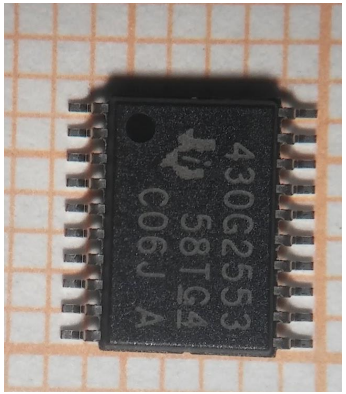


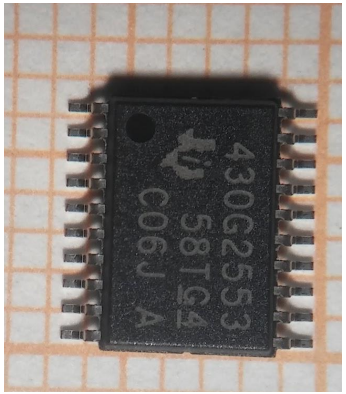
Table 1. Available Options[1][2]

Device	BSL	EEM	Flash (KB)	RAM (B)	Timer_A	COMP_A+ Channel	ADC10 Channel	USCI_A0, USCI_B0	Clock	I/O	Package Type
MSP430G2553IRHB32	1	1	16	512	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2553IPW28										24	28-TSSOP
MSP430G2553IPW20										16	20-TSSOP
MSP430G2553IN20										16	20-PDIP

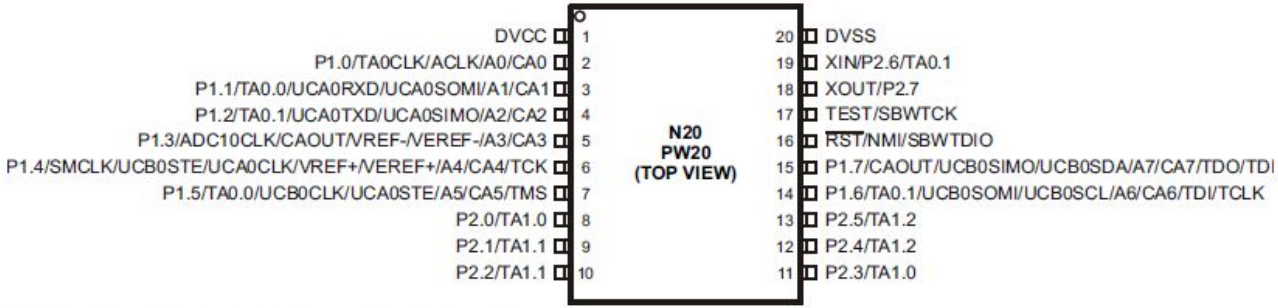
FEATURES

- Low Supply-Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 230 µA at 1 MHz, 2.2 V
  - Standby Mode: 0.5 µA
  - Off Mode (RAM Retention): 0.1 µA
- Five Power-Saving Modes
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 µs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequency
  - Internal Very-Low-Power Low-Frequency (LF) Oscillator
  - 32-kHz Crystal
  - External Digital Clock Source
- Two 16-Bit Timer_A With Three Capture/Compare Registers
- Up to 24 Capacitive-Touch Enabled I/O Pins
- Universal Serial Communication Interface (USCI)
  - Enhanced UART Supporting Auto Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I²C™
- On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion
- 10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan (See Table 1)
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- On-Chip Emulation Logic With Spy-Bi-Wire Interface
- Family Members are Summarized in Table 1
- Package Options

Microprocesadores MSP430

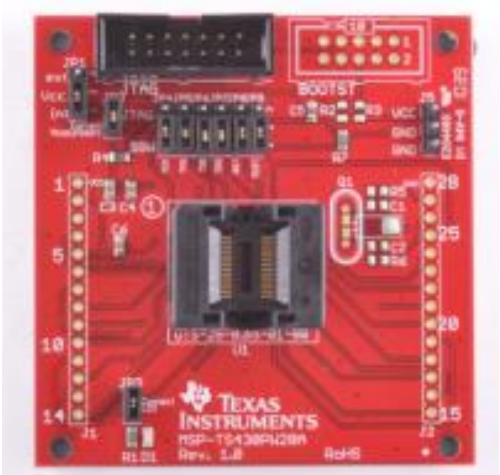


Device Pinout, MSP430G2x13 and MSP430G2x53, 20-Pin Devices, TSSOP and PDIP



NOTE: ADC10 is available on MSP430G2x53 devices only.

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.0/					General-purpose digital I/O pin
TA0CLK/					Timer0_A, clock signal TACLK input
ACLK/	2	2	31	I/O	ACLK signal output
A0					ADC10 analog input A0[1]
CA0					Comparator_A+, CA0 input


JTAG
BOOTST
TEXAS
INSTRUMENTS


TEXAS
INSTRUMENTS
MSP430

Hello world: blinking led

Ingredientes:

1) LED: output digital

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.0/					General-purpose digital I/O pin
TA0CLK/					Timer0_A, clock signal TACLK input
ACLK/	2	2	31	I/O	ACLK signal output
A0					ADC10 analog input A0[1]
CA0					Comparator_A+, CA0 input

8.2.5 *Function Select Registers PxSEL and PxSEL2*

Port pins are often multiplexed with other peripheral module functions. See the device-specific data sheet to determine pin functions. Each PxSEL and PxSEL2 bit is used to select the pin function - I/O port or peripheral module function.

Table 8-1. PxSEL and PxSEL2

PxSEL2	PxSEL	Pin Function
0	0	I/O function is selected.
0	1	Primary peripheral module function is selected.
1	0	Reserved. See device-specific data sheet.
1	1	Secondary peripheral module function is selected.

8.2.2 *Output Registers PxOUT*

Each bit in each PxOUT register is the value to be output on the corresponding I/O pin when the pin is configured as I/O function, output direction, and the pullup/down resistor is disabled.

Bit = 0: The output is low

Bit = 1: The output is high

8.2.3 *Direction Registers PxDIR*

Each bit in each PxDIR register selects the direction of the corresponding I/O pin, regardless of the selected function for the pin. PxDIR bits for I/O pins that are selected for other functions must be set as required by the other function.

Bit = 0: The port pin is switched to input direction

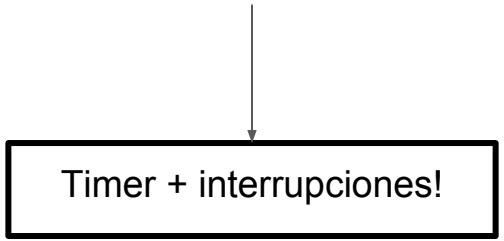
Bit = 1: The port pin is switched to output direction

Hello world: blinking led

Ingredientes:

1) LED: output digital
2) Timing: ¿cómo cuento tiempo?

__delay_cycles(n); ~ wait de python → Mala idea en general



Interrupciones

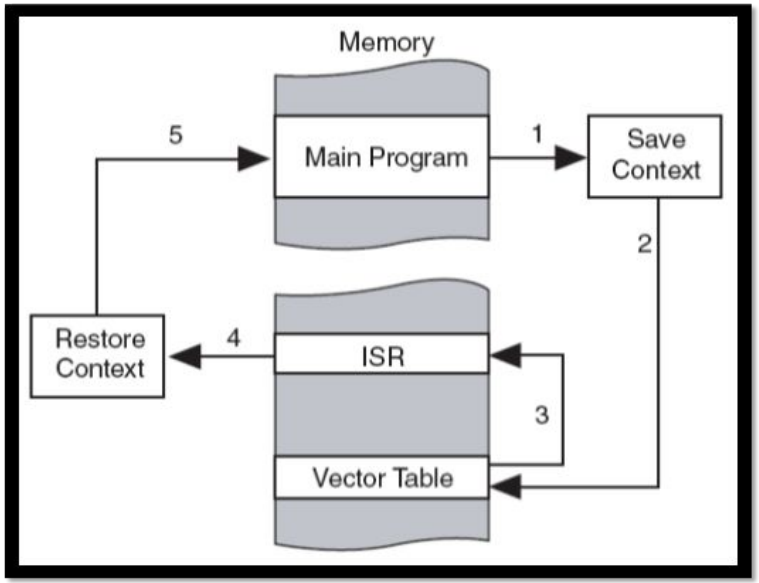


Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range (1)	PORIFG RSTIFG WDTIFG KEYV (2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (2) (3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG (4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG (2) (4)	maskable	0FFF8h	28
Comparator_A+	CAIFG (4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG (4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5) (4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG (2) (5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG (2) (6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG (4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7 (2) (4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7 (2) (4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

Hello world: blinking led

12.3.1 TACTL, Timer_A Control Register

15	14	13	12	11	10	9	8
Unused						TASSELx	
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

7	6	5	4	3	2	1	0
IDx		MCx		Unused	TACLR	TAIE	TAIFG
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)

Unused	Bits 15-10	Unused
TASSELx	Bits 9-8	Timer_A clock source select 00 TACLK 01 ACLK 10 SMCLK 11 INCLK (INCLK is device-specific and is often assigned to the inverted TBCLK) (see the device-specific data sheet)
IDx	Bits 7-6	Input divider. These bits select the divider for the input clock. 00 /1 01 /2 10 /4 11 /8
MCx	Bits 5-4	Mode control. Setting MCx = 00h when Timer_A is not in use conserves power. 00 Stop mode: the timer is halted. 01 Up mode: the timer counts up to TACCR0. 10 Continuous mode: the timer counts up to 0FFFFh. 11 Up/down mode: the timer counts up to TACCR0 then down to 0000h.
Unused	Bit 3	Unused
TACLR	Bit 2	Timer_A clear. Setting this bit resets TAR, the clock divider, and the count direction. The TACLR bit is automatically reset and is always read as zero.
TAIE	Bit 1	Timer_A interrupt enable. This bit enables the TAIFG interrupt request. 0 Interrupt disabled 1 Interrupt enabled
TAIFG	Bit 0	Timer_A interrupt flag 0 No interrupt pending 1 Interrupt pending

5.3.1 DCOCTL, DCO Control Register

7	6	5	4	3	2	1	0
DCOx			MODx				
rw-0	rw-1	rw-1	rw-0	rw-0	rw-0	rw-0	rw-0

DCOx	Bits 7-5	DCO frequency select. These bits select which of the eight discrete DCO frequencies within the range defined by the RSELx setting is selected.
MODx	Bits 4-0	Modulator selection. These bits define how often the f_{DCO+1} frequency is used within a period of 32 DCOCLK cycles. During the remaining clock cycles (32-MOD) the f_{DCO} frequency is used. Not useable when DCOx = 7.

5.3.2 BCSCTL1, Basic Clock System Control Register 1

7	6	5	4	3	2	1	0
XT2OFF	XTS (1)(2)	DIVAx		RSELx			
rw-(1)	rw-(0)	rw-(0)	rw-(0)	rw-0	rw-1	rw-1	rw-1

XT2OFF	Bit 7	XT2 off. This bit turns off the XT2 oscillator 0 XT2 is on 1 XT2 is off if it is not used for MCLK or SMCLK.
XTS	Bit 6	LFXT1 mode select. 0 Low-frequency mode 1 High-frequency mode
DIVAx	Bits 5-4	Divider for ACLK 00 /1 01 /2 10 /4 11 /8
RSELx	Bits 3-0	Range select. Sixteen different frequency ranges are available. The lowest frequency range is selected by setting RSELx = 0. RSEL3 is ignored when DCOR = 1.

Conversor analógico digital de 10 bits (ADC10)

1) Registra señales y devuelve un número de 10 bits (y tengo que hacer algo con esto!)
2) Configurar inicio, reloj, referencia, rango, sample and hold time …
3) Genera una interrupción cuando termina

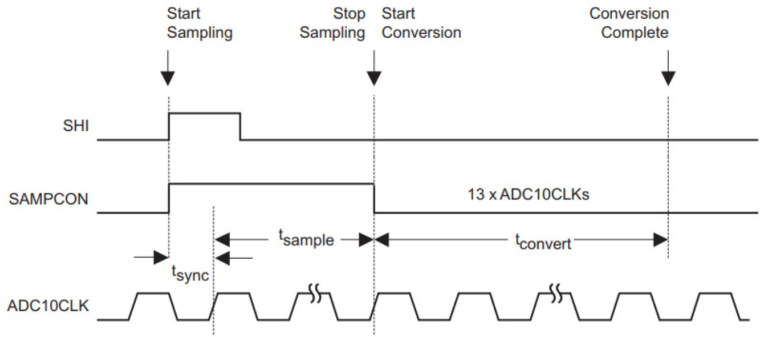
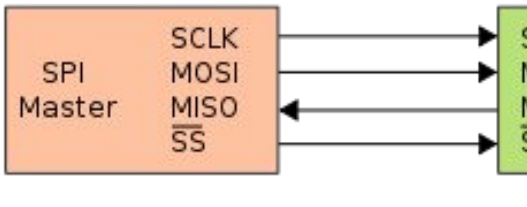
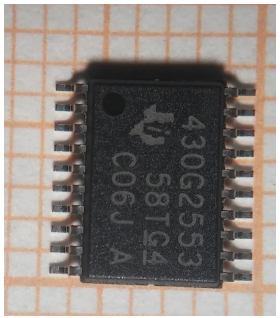


Figure 22-3. Sample Timing

Comunicación con la tarjeta microSD: protocolo SPI

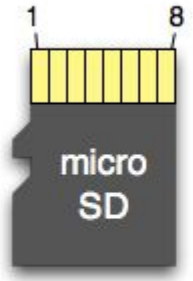
- **S**erial **P**eripheral **I**nterface (SPI) es un protocolo de comunicación sincrónica.
- Soportado por SD (**S**ecure **D**igital)





SPI Bus Mode

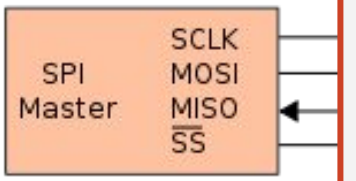
			microSD Pin	Name	I/O	Logic	Description
			2	nCS	I	PP	SPI Card Select [CS] (Negative logic)
			3	DI	I	PP	SPI Serial Data In [MOSI]
				VSS	S	S	Ground
4	4	4	4	VDD	S	S	Power
5	5	5	5	CLK	I	PP	SPI Serial Clock [SCLK]
6	6	6	6	VSS	S	S	Ground
7	7	7	7	DO	O	PP	SPI Serial Data Out [MISO]
	8	8	8	NC nIRQ	. O	. OD	Unused (memory cards) Interrupt (SDIO cards) (Negative logic)
	9	9	1	NC	.	.	Unused
		10		NC	.	.	Reserved
		11		NC	.	.	Reserved

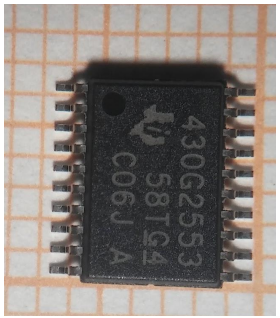


Comunicación con la tarjeta microSD: protocolo SPI

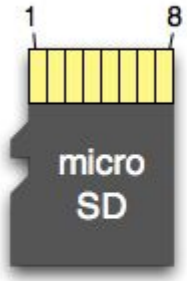
- **S**erial **P**eripheral **I**nterface (SPI) es un protocolo de comunicación sincrónica.
- Soportado p

Alguien ya lo programó!

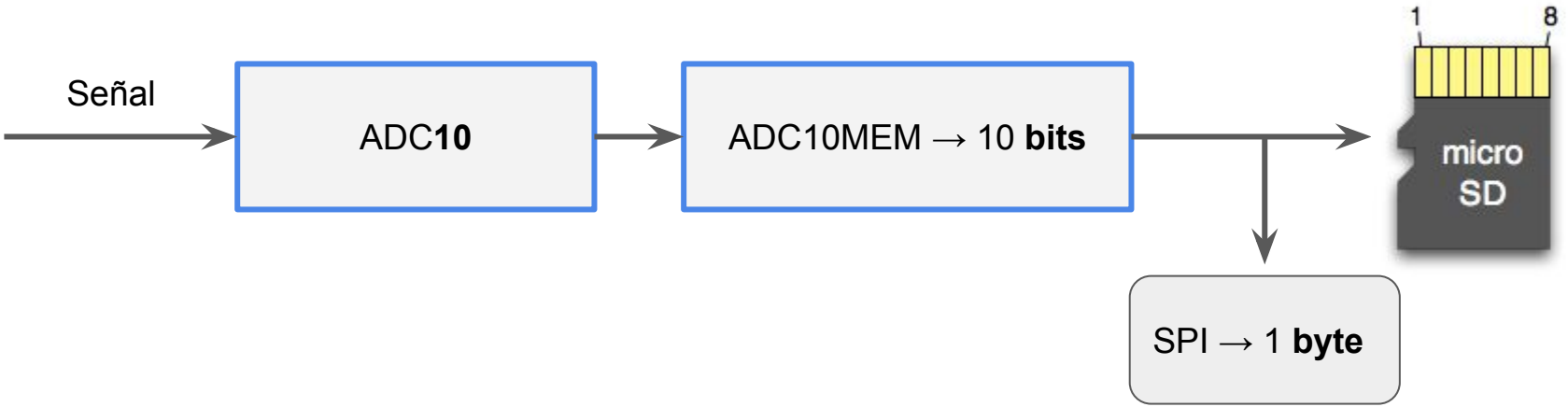




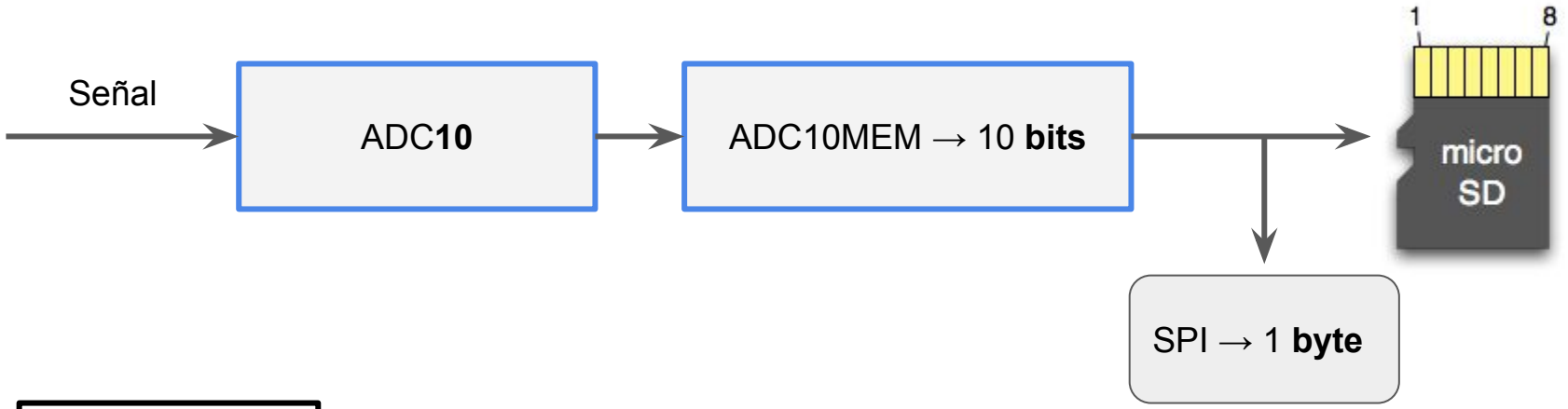
							Description
							rd Select [CS] (Negative logic)
							rial Data In [MOSI]
							d
4	4	4	4	VDD	S	S	Power
5	5	5	5	CLK	I	PP	SPI Serial Clock [SCLK]
6	6	6	6	VSS	S	S	Ground
7	7	7	7	DO	O	PP	SPI Serial Data Out [MISO]
	8	8	8	NC nIRQ	. O	. OD	Unused (memory cards) Interrupt (SDIO cards) (Negative logic)
	9	9	1	NC	.	.	Unused
		10		NC	.	.	Reserved
		11		NC	.	.	Reserved



Resolución vs sampleo: 8 bits o 10 bits?



Resolución vs sampleo: 8 bits o 10 bits?

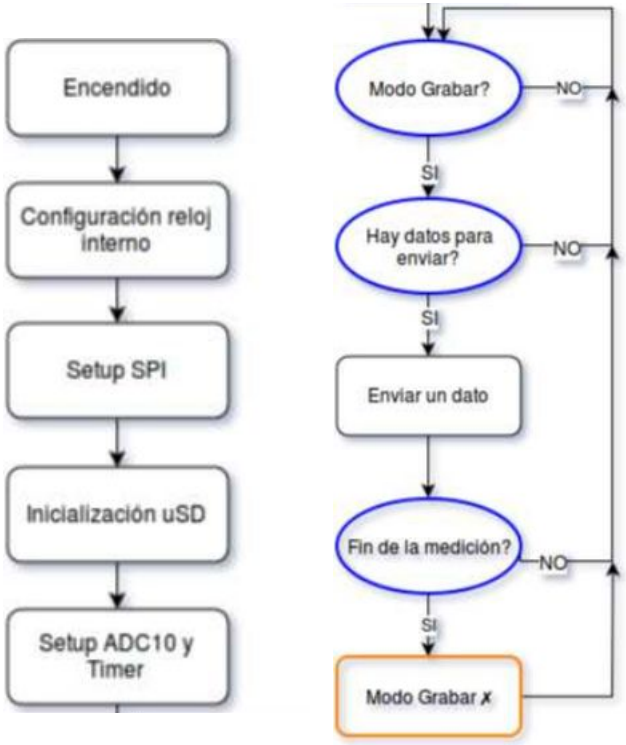


0V = 0
3.7V = 1023

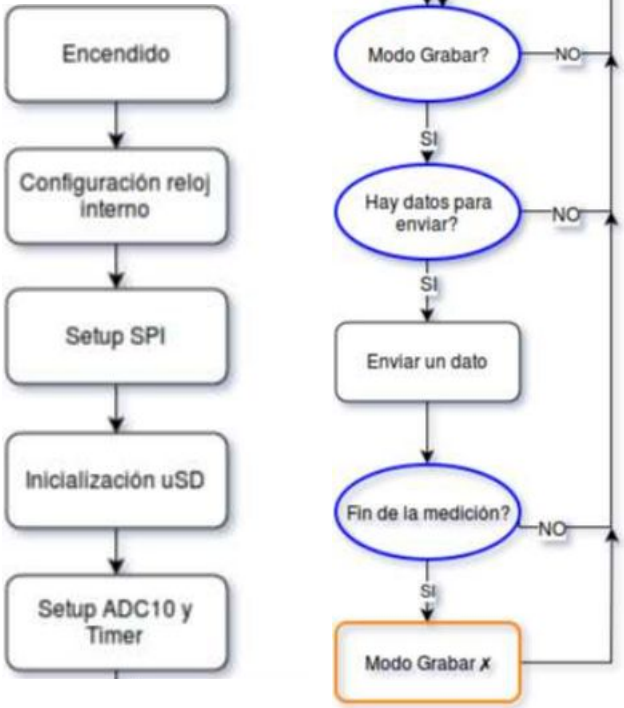
1.92V → 530 = 10 0001 0010 → 1000 0100 + 10

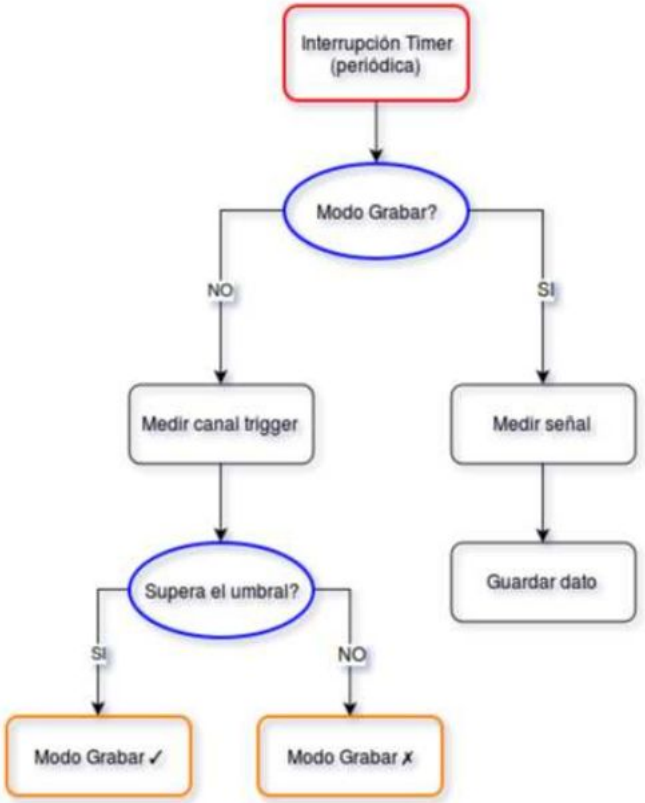
- Envío 8 bits
- Envío 8 bits + 2 bits

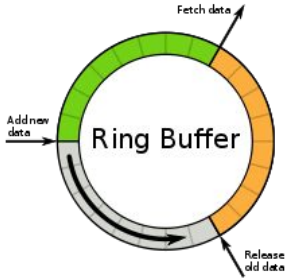
Flujo del programa



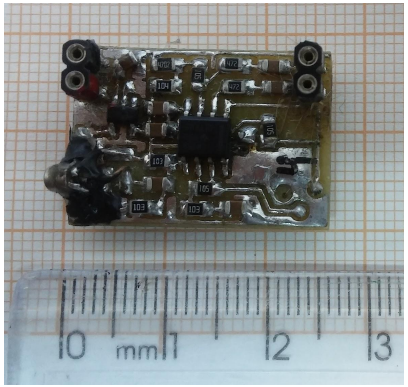
Flujo del programa

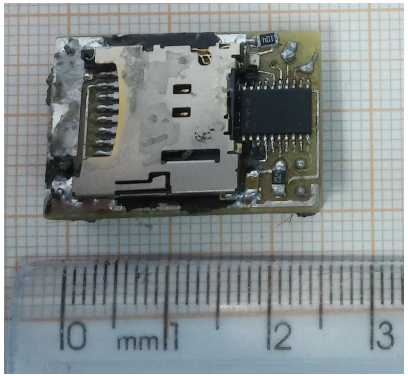






Problemas y desafíos





- Abrir archivos es muy lento: escribimos directamente en bytes
- Hay que saber cómo se grabaron los datos para poder leerlos
- Muy poco RAM: 512 bytes
- El manejo de la tarjeta limita la frecuencia de adquisición
- Tiempos muertos y lo que los fabricantes no dicen, ruidos y demás
- Baterías LiPo (de peso razonable) permiten ~7hs de adquisición continua

¡Gracias!