REPORT

DEVICE TECHNOLOGY

Scaling carbon nanotube complementary transistors to 5-nm gate lengths

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High-performance top-gated carbon nanotube field-effect transistors (CNT FETs) with a gate length of 5 nanometers can be fabricated that perform better than silicon complementary metal-oxide semiconductor (CMOS) FETs at the same scale. A scaling trend study revealed that the scaled CNT-based devices, which use graphene contacts, can operate much faster and at much lower supply voltage (0.4 versus 0.7 volts) and with much smaller subthreshold slope (typically 73 millivolts per decade). The 5-nanometer CNT FETs approached the quantum limit of FETs by using only one electron per switching operation. In addition, the contact length of the CNT CMOS devices was also scaled down to 25 nanometers, and a CMOS inverter with a total pitch size of 240 nanometers was also demonstrated.

Silicon complementary metal-oxide semiconductor (CMOS) technology will soon reach its performance limits at the sub–10 nm technology node (*1*–*7*). Semiconducting single-wall carbon nanotube (s-SWCNT)–based field-effect transistors (FETs) have been considered for sub–10 nm technology nodes because of their nanoscale dimensions, high carrier mobility, and excellent stability (*4*, *8*, *9*), which in principle could provide much better scaling properties and improved on-state performance than CMOS FETs based on Si and other semiconductors (e.g., Ge or InGaAs with the same gate length) (*10*–*14*). Carbon nanotube (CNT)–based CMOS FETs have been fabricated and shown to possess certain advantages over Si CMOS FETs with channel lengths greater than 50 nm (*15*, *16*) and have been scaled down to 20 nm using a gate-all-around structure, albeit with limited performance (*17*). Moreover, excellent scaling behavior has been demonstrated down to 9 nm for p-type FETs with a simple local back-gate structure (*18*, *19*). However, sub–10 nm CNT CMOS FETs have not been reported, and no unambiguous performance advantage has been shown over state-of-the-art Si CMOS FETs for sub–10 nm technology nodes. Although the ultimate performance of CNT-based CMOS FETs has been assessed (*8*), these studies are based mainly on theoretical simulations or extrapolations from experimental results obtained for larger devices.

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We report the fabrication of high-performance CNT CMOS FETs with a gate length scaled down to <10 nm using a doping-free process and a top gate structure, and we explore the scaling behavior and potential of CNT FETs. The scaled CNT CMOS FETs exhibited higher intrinsic performance and lower power consumption than Si CMOS FETs with a similar gate length but at a lower supply voltage (V_{dd}). At the 5-nm gate length, although CNT FETs with an excellent on-state performance can be fabricated with conventional metal contacts, the off-state properties of these devices are generally compromised. Graphene-contacted CNT FETs are thus proposed and demonstrated to feature a slightly reduced on-state current but a substantially improved off-state performance. We then explore the contact length scaling behavior for CNT CMOS FETs and present a CMOS inverter with a total pitch size of 240 nm, which is smaller than that of Si at the 22-nm technology node. Our results show that CNT CMOS technology can yield FETs with a performance that approaches that of an ultimate binary switch with limits imposed by thermodynamics and quantum mechanics.

To explore the scaling limit of CNT FETs, we used individual s-SWCNTs to construct FETs. Although this type of material is not suitable for building large-scale integrated circuits (ICs), it is well defined and most appropriate for exploring the scaling limit of CNT FETs because devices with different channel lengths but identical material parameters can be fabricated on the same s-SWCNT. A similar approach has been used for investigating gate length and contact scaling (*17*–*19*). We used a well-developed doping-free process to fabricate complementary FETs on preselected s-SWCNTs with a top gate structure (*11*, *15*). The structure and fabrication process flow of the CNT CMOS FETs are shown in fig. S1, together with three cross-sectional transmission electron microscopy (TEM) images (Fig. 1A) showing a p-type FET, an n-type FET, and the gate stack structure of these devices. The transfer (Fig. 1B) and output (fig. S2C) characteristics are shown for a pair of 10-nm CMOS FETs fabricated on the same s-SWCNT. A subthreshold slope (SS) of 70 mV/decade was obtained for both n-type and p-type FETs [the requirement on SS is smaller than 80 mV/decade for commercial Si CMOS devices] and was much lower than that of previously reported short-channel p-type CNT FETs [larger than 90 mV/decade for 9-nm p-FET] (*19*), indicating excellent gate control from the top gate on the 10-nm CNT channel beneath the gate. This electrostatic potential control on the conducting channel in our devices was enabled by the ultrathin body of the CNT and the highly efficient gate with ultrathin HfO_2 of 3.5 nm (Fig. 1A) (*20*). The n-type and p-type FETs in Fig. 1 exhibit nearly symmetric performance because of the symmetry in both mobility and injection efficiency between electrons and holes in the CNTs (*15*). Large transconductances were also achieved in both n-type and p-type FETs, and we observed up to 55 μS per CNT for the n-type FET (fig. S2A), compared with 45 μS per CNT for previously reported n-type CNT FETs [(*21*), gate-all-around structure] and comparable to that of the highest-performing p-type FETs (55 μS per CNT) (*19*). At a relatively low bias of 0.4 V, the on-state current I_{ds} is as high as 17.5 μA for the p-type FET and 20 μA for the n-type FET (Fig. 1B and fig. S2C), demonstrating the potential for low-power applications with very low supply voltage (e.g., 0.4 V). The on-state performance originates primarily from the perfect ohmic contacts and is manifested in the high output conductance of more than 0.5 G_0 at low bias (where G_0 is the quantum limit for conductance of a s-SWCNT) for both n-type and p-type FETs (fig. S2A).

To evaluate the relative performance of CNT CMOS FETs against that of their Si counterparts, we compared typical transfer characteristics of CNT CMOS FETs to those of Intel's 14- and 22-nm Si CMOS FETs, which are the highest-performing FETs reported to date (*22*, *23*). The direct comparison between CNT and Si CMOS FETs is shown in Fig. 1, C and D, in which the current density of CNT FETs is normalized by assuming 125 CNTs/μm (*24*, *25*). The 10-nm CNT CMOS FETs exhibited higher on-state current even at a much smaller supply voltage than that of the Si CMOS FETs (0.4 V versus 0.7 and 0.8 V), as well as smaller average SS than Si CMOS FETs. Quantitatively, 10-nm CNT CMOS FETs powered at 0.4 V can provide comparable on-state current with that of state-of-the-art Si CMOS FETs at the 14-nm technology node powered at 0.7 V; lowering the supply voltage while maintaining or even improving performance is the primary goal for scaling down transistors (*3*, *4*).

Although both high on-state performance and low SS have been demonstrated in 10-nm CNT CMOS FETs, there remains a potential obstacle for the application of these CNT FETs in low-power

ICs, namely, the relatively large off-state current arising from the small band gap and small effective mass of carriers in CNTs. This off-state current can, however, be reduced by using s-SWCNTs with diameters in the range of 1 nm or less and by using an asymmetric source and drain structure (*8*, *26*, *27*). Challenges remain to suppress the ambipolar conduction in larger s-SWCNTs, to form ohmic contacts to small s-SWCNTs with diameters of 1 nm or less, and to implement asymmetric device geometry for extremely scaled CNT FETs. In addition, further improvement of SS and an increase in the threshold voltage V_{th} can also help to lower the off-state current. Trade-offs should be made between high performance and off-state power dissipation in a device, particularly for sub–10 nm CNT CMOS FETs. In general, large diameters and short channels are appropriate for high performance, and small diameters and asymmetric device structure are appropriate for low-power applications.

To explore the scaling limits of CNT FETs (*3*, *7*, *8*, *28*), we considered scaling down the gate length of the CNT FET to 5 nm (Fig. 2). The TEM image shown in Fig. 2A reveals that the gate length of the CNT FET is ~5 nm. At this length scale, the FET with a highly efficient top gate still exhibited excellent field-effect characteristics (fig. S3, B to D), with an ultrasmall output resistance of 10 kilohms at low bias and a large saturated current of ~20 μA at a bias of 0.4 V (fig. S3E). This large on-state current arose because the effective channel length of the device was smaller than the mean free path determined by optical phonon scattering (between 10 and 15 nm) in the CNT channel (*29*, *30*), which also leads to a very high room-temperature linear conductance of up to 0.64 G_0. However, the 5-nm CNT FET suffered from a degraded SS ranging from 105 to 130 mV/decade (fig. S3B), which is much higher than that of 10- to 20-nm FETs (fig. S2D). Thus, the top gate structure with an effective oxide thickness as small as 1.05 nm could not provide sufficient gate control as the gate length was scaled down to 5 nm. A relatively large contact thickness led to non-negligible screening against the gate control of the channel. This phenomenon, referred to as the short-channel effect, occurred because in an ultrashort channel FET, the drain began to share the electrostatic potential control of the channel with the gate; ultimately, the degradation of SS will be caused by direct tunneling between the source and drain electrodes (*31*).

To maintain the control of the channel by the gate, the scaling of the FET should be carried out both laterally on the channel length and vertically on the gate dielectric and channel thickness (*3*–*5*). However, the extremely downscaled thicknesses of the gate dielectric and channel body are not sufficient to provide enough gate control in 5-nm FETs, and a thinner source and drain are necessary to maintain electrostatic gate control of the channel (see the simulated results in fig. S4) (*32*, *33*). Thus, we used the thinnest conducting material, graphene, as the source/drain electrode for sub–10 nm CNT FETs to improve electrostatic control of the gate by reducing the parasitic capacitance of the source/drain to the channel. The schematic structure and electron microscopy images of the graphene-contacted (GC) CNT FET are shown in Fig. 2, A and B, and fig. S5, and detailed fabricated processes are given in the supplement and in figs. S6 and S7. The transfer characteristics of seven GC CNT FETs with L_g = 10 nm exhibited SS with an average value of 66 mV/decade (Fig. 2D and fig. S5C), and the best SS value was near the theoretical limit of 60 mV/decade at room temperature. When the channel length was further scaled down to 5 nm, the introduction of the ultrathin graphene source/drain improved the gate efficiency (Fig. 2E); a typical SS value was 73 mV/decade, which is substantially better than the SS of a typical 5-nm Si MOS FET (208 mV/decade) (*34*).

The operational principle of the top-gate GC FET differs from that of the conventional FET in that the gate not only controls the CNT channel but also modulates the carrier density of the graphene source/drain regions beneath the gate.

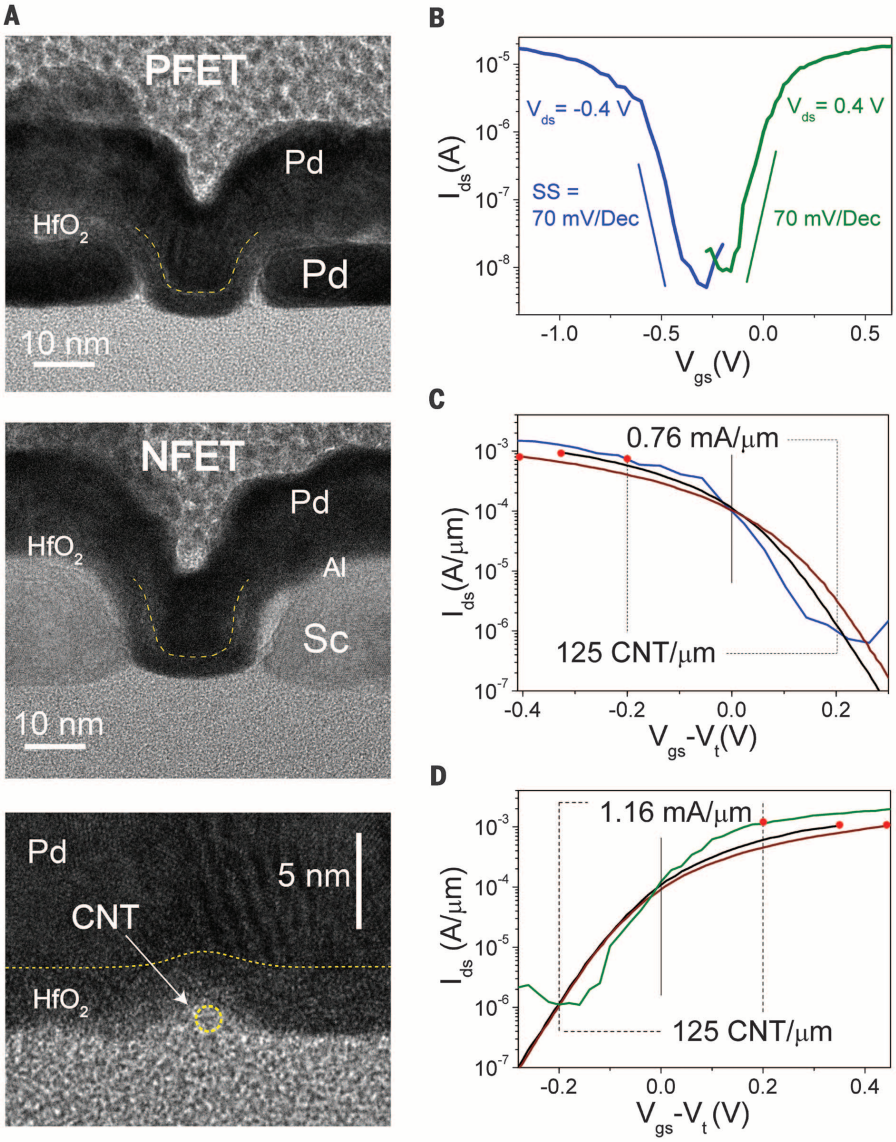

Fig. 1. Structure and performance of 10-nm CNT CMOS FETs. (**A**) TEM images showing the cross sections of a p-type FET, n-type FET, and gate stack; gate length 10 nm, channel length 20 nm. (**B**) Transfer characteristics (drain current I_{ds} versus gate voltage V_{gs}) of typical CMOS FETs fabricated on a s-SWCNT with a diameter of 1.3 nm at a drain bias V_{ds} = ±0.4 V. The solid blue and olive curves represent CNT p-type and n-type FETs, respectively. (**C** and **D**) Comparison of 10-nm CNT CMOS FETs and commercial Si CMOS transistors of Intel's 14-nm (*22*) (solid black curve) and 22-nm nodes (*23*) (solid maroon curve). The on-currents of n-FETs for CNT, Si 14-nm node, and Si 22-nm node are 1.16 mA/μm (V_{dd} = 0.4 V, 125 CNTs/μm), 1.1 mA/μm (V_{dd} = 0.7 V), and 1.03 mA/μm (V_{dd} = 0.8 V), respectively. The on-currents of p-FETs for CNT, Si 14-nm node, and Si 22-nm node are 0.76 mA/μm (V_{dd} = 0.4 V, 125 CNTs/μm), 0.96 mA/μm (V_{dd} = 0.7 V), and 0.83 mA/μm (V_{dd} = 0.8 V), respectively. CNT CMOS FETs and 14- and 22-nm Si CMOS FETs have gate lengths of 10 nm, 20 nm, and 26 to 30 nm, respectively. The contact length of CNT CMOS FETs was not scaled.

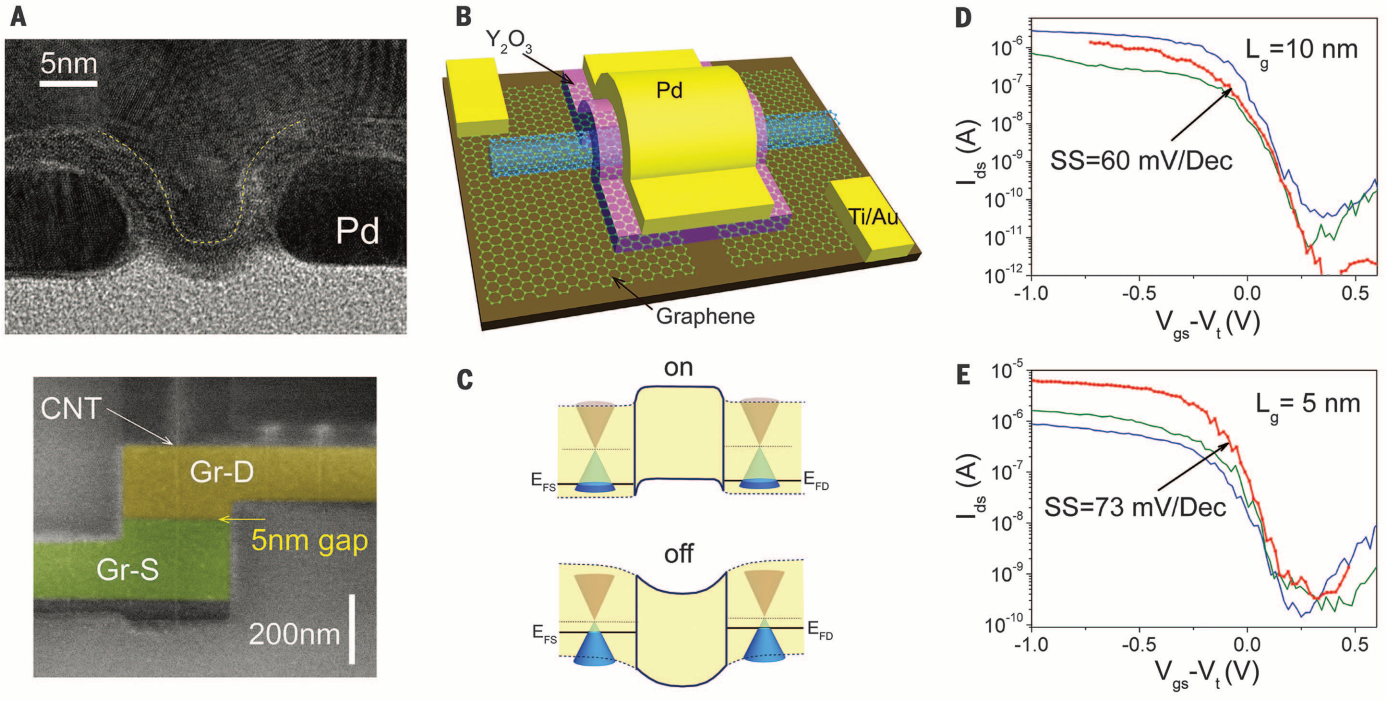

Fig. 2. Structure and performance of 5-nm CNT FETs. (**A**) Top: TEM image of a normal Pd-contacted CNT FET with gate length of 5 nm. Bottom: SEM image of a graphene-contacted CNT FET with channel length of 5 nm, before the deposition of the top gate electrode. (**B**) Schematic diagram showing the structure of a GC CNT FET. (**C**) Schematic band diagrams of the graphene-contacted CNT FET in its on-state (top) and off-state (bottom). E_{FS} and E_{FD} are the Fermi levels of source and drain graphene electrodes, respectively. (**D**) Transfer characteristics of three typical GC CNT FETs with L_g = 10 nm and a typical SS of 60 mV/decade at V_{ds} = −0.1 V. (**E**) Transfer characteristics of three typical GC CNT FETs with L_g = 5 nm and a typical SS of 73 mV/decade at V_{ds} = −0.1 V.

A numerical simulation for the short-channel CNT FETs with a Pd local back-gate geometry showed that the back gate strongly modulated the contact properties, allowing for the realization of superior subthreshold swings for short-channel devices (*35*). In addition, the weak electrostatic screening of graphene helps to enhance the gate controllability on the CNT channel between the graphene contacts, thus reducing the short-channel effect (fig. S4). When the device is switched to its on-state, the GC FET becomes a ballistic FET with a 5-nm channel (Fig. 2C, top). On the other hand, when in its off-state, part of the CNT outside the 5-nm channel but below the gate is also depleted by the gate; the gate-induced barrier thus becomes broader than the channel length, leading to suppression of direct tunneling between the source and drain or improved off-state performance (Fig. 2C, bottom).

An ideal high-performance FET should exhibit a large on-state current I_{on}, small off-state current I_{off}, and small SS for fixed gate length L_g and supply voltage V_{dd}. We compared the performance of our CNT CMOS FETs with that of the highest-performing small CNT FETs (Fig. 3A). I_{on} is defined as the current at $|V_{gs} - V_{th}|$ = 0.4 V for a supply voltage of $|V_{dd}|$ = 0.4 V (*17*). Figure 3A shows that our CNT CMOS FETs can typically provide I_{on} values in the range of 5 to 15 μA, which is much larger than most of the published CNT FETs with a similar or smaller L_g (*17*–*19*, *36*). The scaling of SS with L_g of our CNT CMOS FETs (Fig. 3B) also compares favorably with the best reported FETs, including CNT FETs and state-of-the-art silicon CMOS FETs (*17*–*19*, *22*, *23*, *36*–*38*). In particular, some of our CNT CMOS FETs exhibited very small SS even when being scaled down to 5 nm, which we attributed to the improved gate control on the channel and suppressed direct tunneling between the source and drain. The scaling trend of SS of our CNT CMOS FETs is obviously better [SS about 73 mV/decade versus beyond 100 mV/decade for 5-nm gate length] than that of planar Si MOS FETs and FinFETs (*37*).

To benchmark CMOS FETs based on CNTs and Si, we used the Intel methodology and key device metrics, including intrinsic gate delay (a measure of intrinsic speed) and energy-delay products (EDPs, a measure of switching energy) (*37*). Both p-type and n-type CNT FETs exhibited smaller intrinsic gate delays than that of the corresponding Si FETs with a 10-nm gate length by a factor of ~5 to 10; however, a very small V_{dd} of 0.4 V was used for the CNT FETs, whereas a much larger V_{dd} of 0.7 V was used for the Si devices (Fig. 3C and fig. S8A). In particular, the intrinsic gate delays of the CNT devices were 90 and 57 fs for the 10-nm p-type and n-type FETs, respectively, and this delay was further reduced to 43 fs for the 5-nm p-type CNT FETs. In comparison, the ultimate intrinsic gate delay for Si FETs is projected to be 100 fs by the 2013 International Technology Roadmap for Semiconductors (ITRS) in 2026 for the Si FET with L_g = 5.9 nm (*39*). The realized gate delay of 43 fs in the 5-nm CNT FET is already near that of the theoretical speed limit of a binary switch determined by the Heisenberg uncertainty principle (*4*, *6*, *40*, *41*). Figure 3D and fig. S8B show the scaling trends of the CNT and Si CMOS FETs in terms of the EDP, which is usually used to benchmark the available parameter space when considering trade-offs between speed and dynamic power in designing a transistor. The EDP in CNT CMOS FETs is lower than that in Si CMOS FETs by approximately an order of magnitude for the same L_g. The 10-nm CNT CMOS FETs exhibit EDPs as low as 1.88×10^{-30} Js/μm, which is substantially lower than the predicted limit of a Si n-type FET at the end of ITRS (*39*). The performance advantages of CNT CMOS FETs over Si CMOS FETs mainly originate from the smaller intrinsic gate capacitance, thin body, and higher carrier mobility of the CNT channel. Additionally, the lower V_{dd} increases the advantageous EDP for CNT CMOS by a factor of ~10 relative to that of Si CMOS devices with the same gate length.

As an irreversible binary switch, the scaling of the FET will eventually reach an absolute performance limit given by the Shannon–von Neumann–Landauer (SNL) expression and the uncertainty principle (*4*, *6*). Indeed, the gate length, intrinsic gate delay, and EDP of our 10-nm and 5-nm CNT FETs are already near the corresponding theoretical limits of a binary switch (*6*). In particular, the gate delay of the 5-nm CNT FET is scaled down to 43 fs, which should be compared with the theoretical limit of 40 fs. Table 1 also

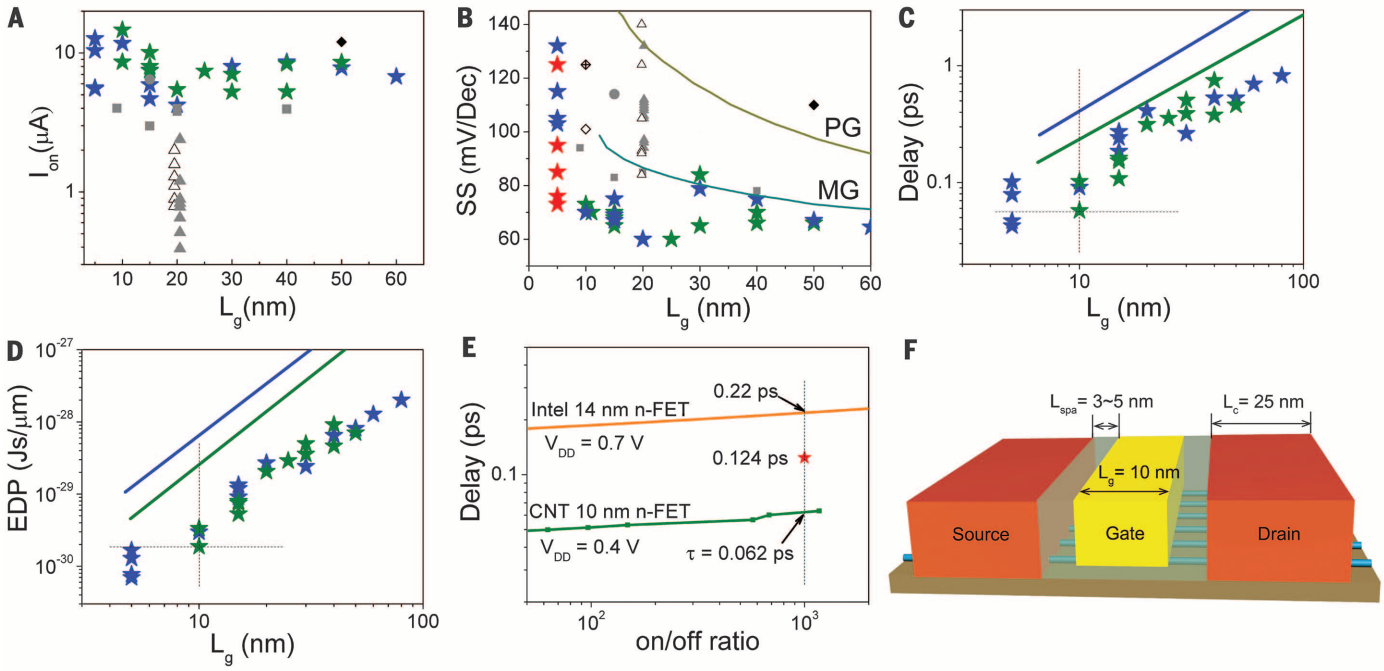

Fig. 3. Benchmarking CNT CMOS FETs in this work with published CNT FETs and Si CMOS FETs. (**A**) Comparison of the on-state currents of various sub–100 nm CNT FETs (*13*, *17*–*19*, *36*). I_{on} values of all published CNT FETs are extracted for V_{ds} = 0.4 V and $V_{gs} - V_t$ = 0.4 V, where V_t is the threshold voltage (*17*). (**B**) Scaling characteristics of the subthreshold slopes for CNT and Si CMOS FETs (*37*, *38*). The dark yellow curve represents Si planar-gate (PG) MOS FETs; the dark cyan curve represents multigate (MG) Si MOS FETs (*37*). In (A) and (B), gray squares denote back-gate p-type FETs (*18*, *19*), gray dots and black diamonds denote top-gate p-type FETs (*13*, *36*), open triangles denote GAA p-type FETs, and solid triangles denote GAA n-type FETs (*17*). (**C** and **D**) Scaling trends of the gate delay and EDP of CNT CMOS FETs compared to that of Si CMOS FETs (*37*, *39*). The blue solid line represents the fitting of experiment data of Si p-type MOS FETs (*37*); the olive solid line represents Si n-type MOS FETs (*37*). All data for CNT CMOS FETs are evaluated at V_{dd} = 0.4 V. In all panels, blue and olive stars represent p-type and n-type CNT FETs, respectively; red stars in (B) represent graphene-contacted CNT FETs. (**E**) Intrinsic gate delay versus current on/off ratio for a 10-nm CNT n-type FET (green line) at V_{dd} = 0.4 V and a comparison with Si n-type FETs (orange line) at the 14-nm technology nodes and V_{dd} = 0.7 V (*22*). The intrinsic gate delay of the Si and CNT FETs does not include the influence of parasite capacitances. Red star in (E) represents evaluated delay for a scaled n-type CNT FET with a pitch of 45 nm and structure as in (F). (**F**) Structure with gate length of 10 nm and contact length of 25 nm; L_{spa} is the thickness of the spacer between the gate and source (or drain).

shows that, on average, there are only 1.35 electrons in the 5-nm CNT channel in its on-state, which suggests that typically only one electron is involved during the switching of the 5-nm CNT FET. Benefiting from the outstanding electrical properties and small intrinsic gate capacitance, the 10-nm CNT CMOS FETs display ultrasmall intrinsic gate delays (Fig. 3E) at 0.4 V, which are approximately one-third that of 14-nm Si CMOS FETs at 0.7 V with the same current on/off ratio (*22*). The gate delay of our 10-nm CNT CMOS FETs can be reduced to 62 fs (for n-type FETs) for a current on/off ratio of 1000, and further down to the theoretical limit of 40 fs when the current on/off ratio is reduced to 2 (*6*).

A small FET must simultaneously possess a small channel and small contacts to provide a higher packing density, making the contact length scaling equally as important as the channel length scaling. Franklin *et al.* have studied the contact length (L_c) scaling behavior of Pd-contacted back-gate CNT FETs and have shown that the performance of CNT FETs depends strongly on L_c, especially when the contact length is in the sub–100 nm regime (*18*, *28*, *42*). However, the L_c scaling behavior of top-gated CNT FETs and Sc-contacted or n-type CNT FETs has never been investigated. In particular, the scaling of the Sc-contacted n-type FET is an issue of great concern, as it is generally believed that n-type FETs are less stable than p-type FETs. It is thus important to establish whether similar scaling behaviors exist for n-type and p-type contact lengths.

We first consider the Sc contact length scaling for n-type CNT FETs. SEM images of relevant devices are shown in fig. S9B, in which L_c was scaled from 100 nm to 25 nm while maintaining a constant gate length (30 nm) and channel length (50 nm). To prevent the Sc contact from oxidizing in air, the Sc film was covered with a 3-nm Al film. In addition, a gate stack–first fabrication process is adopted to reduce the oxidation of the Sc/Al contact during the fabrication of the gate stack (see fig. S11 and the supplement). We selected two s-SWCNTs with different diameters and fabricated two groups of n-type and p-type FETs with various L_c values for each s-SWCNT. The transfer characteristics of a typical group of FETs based on one s-SWCNT with L_c ranging from 100 nm to 25 nm are presented in Fig. 4A and fig. S10, which show that I_{on} decreased with reducing L_c. The scaling behavior of the contact resistance with the contact length of CNT CMOS FETs is shown in Fig. 4B. For the s-SWCNT with a diameter of 1.1 nm (CNT 1), the contact resistances (R_{S+D}) of both n-type and p-type FETs increased rapidly as L_c was reduced, especially when the contact length was scaled down into the sub–50 nm regime. This rapidly increasing contact resistance is the main obstacle for further pitch size downscaling in CNT CMOS FETs and, in fact, for any CMOS FET downscaling. Using s-SWCNTs with a larger diameter (e.g., CNT 2 with a diameter of 1.5 nm; Fig. 4B) in the FETs considerably improved performance. CMOS FETs fabricated on the large-diameter CNT 2 exhibited unambiguously smaller R_{S+D} than those of the FETs fabricated on the smaller-diameter CNT 1 and exhibited no detectable R_{S+D} degeneration until L_c was reduced to 25 nm. The experimental scaling trend of R_{S+D} is consistent with the theory developed by Wong and co-workers (*28*). It was important to maintain R_{S+D} below 30 kilohms for both n-type and p-type FETs as L_c was scaled down to 25 nm to satisfy the requirement of the 10-nm technology node (*28*). More aggressive downscaling to <10 nm has also been demonstrated by IBM researchers who used

Table 1. Comparison of key device metrics for various FETs and theoretical limits.

	Limit	Si CMOS (10-nm node)	CNT FET (10 nm)	CNT FET (5 nm)
Gate length (nm)	1.5	13.4 to 16.8	10	5
Gate delay (fs)	40	220	57	43
EDP (Js/μm)	—	6.79×10^{-29}	1.88×10^{-30}	6.95×10^{-31}
Carrier density (1/μm)	—	1745	338 (2.7/CNT)	169 (1.35/CNT)

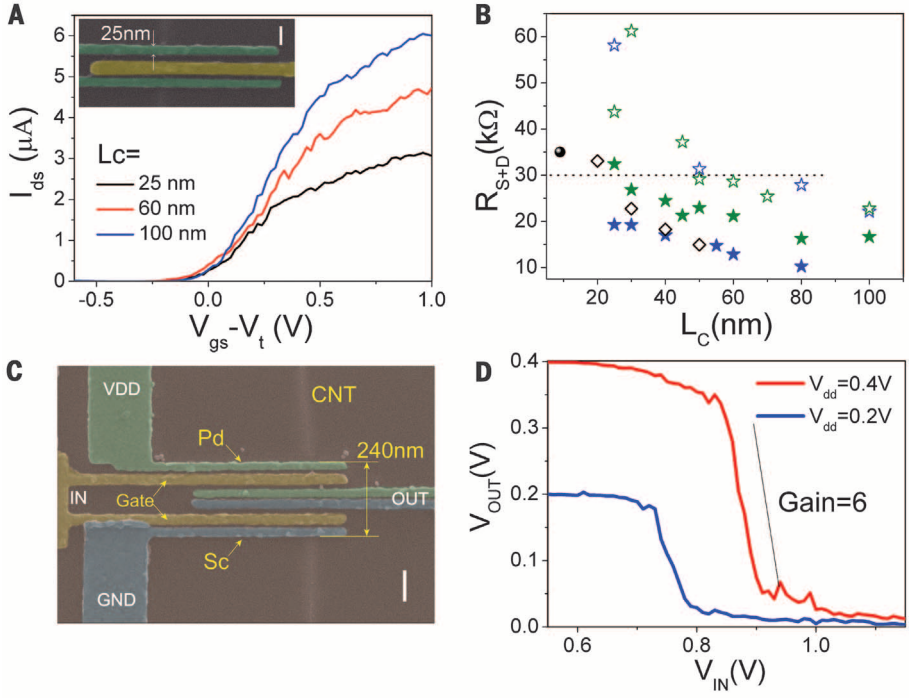

Fig. 4. Contact length scaling of CNT CMOS FETs. (**A**) Transfer characteristics at V_{ds} = 0.1 V for CNT n-type FETs with contact lengths of 100, 60, and 25 nm; inset shows top-view SEM image of a typical CNT n-type FET with contact length of 25 nm. (**B**) Scaling characteristics of contact resistances for both p-type (blue stars) and n-type (olive stars) CNT FETs. Open stars represent FETs based on CNT 1 (diameter ~1.1 nm); solid stars represent FETs based on CNT 2 (diameter ~1.5 nm). Hollow diamonds represent the contact resistances for p-type CNT FETs with Pd side contacts (*42*) and the solid sphere for the Mo end contact (*43*). (**C**) SEM image showing a typical CNT CMOS inverter. The size of the entire inverter is ~240 nm. Scale bar, 100 nm. VDD is the supply voltage. (**D**) Transfer characteristics of the CNT inverter measured with power supply voltages of 0.4 V and 0.2 V.

an end-bonded contact geometry and showed that this method provides good contact for L_c down to 9 nm (*43*). However, the technology developed by IBM works only for p-type FETs, and it remains a challenge to demonstrate end-bonded contacts for n-type FETs. The gate delay projected for a scaled n-type FET is marked in Fig. 3E, with a total pitch size of 45 nm and a structure depicted in Fig. 3F, which also compared favorably to that of the Si 14-nm n-type FET with larger pitch size (70 nm) (*22*).

To demonstrate the construction and operation of scaled CNT CMOS circuits, we consider here the simplest CMOS circuit: a CMOS inverter (Fig. 4, C and D). In this inverter, the Pd and Sc contact lengths were 23 and 27 nm, respectively, and the gate length was ~35 nm for both n-type and p-type CNT FETs. The pitch sizes of the n-type FET and p-type FET were thus 94 and 87 nm, respectively. Unlike Si CMOS ICs, in which an isolation region between n-type and p-type FETs is necessary, no isolation region is required for the CNT CMOS circuit, and the drains of the n-type and p-type CNT FETs can thus be placed together. The reduction in the isolation region between n-type and p-type devices in our doping-free CNT CMOS circuits provides an additional advantage over Si CMOS technology and avoids a considerable number of processing steps and requisite chip area and shortens local interconnects between FETs. As a result, the total pitch size of the CNT CMOS inverter is reduced to 240 nm, which is smaller than that of the Si-based CMOS inverter at the 22-nm technology node (*23*), although the CNT CMOS FETs used here with a gate length of 35 nm are considerably larger than that used in the Si 22-nm technology node. The transfer characteristics in Fig. 4D show that the 240-nm CNT inverter performs well at V_{dd} = 0.4 V and even at 0.2 V, with a sharp voltage transition region and large voltage gain of approximately 6 at V_{dd} = 0.4 V, except for V_{th} mismatch between n- and p-type FETs leading to non–rail-to-rail output of the inverter. In principle, V_{th} can be independently controlled for each FET—for example, by using gate metals of different work functions (*14*)—but this is difficult to realize for extremely scaled CMOS circuits with currently available fabrication facilities in our laboratory.

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ACKNOWLEDGMENTS

We thank J. Su, Y. Gao, and L. Ding from Huazhong University of Science and Technology for TEM technique support; H. Peng and B. Deng from Peking University for supplying CVD-derived graphene samples; and Y. Wu and G. Zhang for useful discussions. Supported by National Key Research and Development Program grants 2016YFA0201901 and 2016YFA0201902; National Science Foundation of China grants 61322105, 61376126, 61621001, and 61427901; and Beijing Municipal Science and Technology Commission grants D151100003315004 and Z151100003315009. Author contributions: L.-M.P. and Z.Z. proposed and supervised the project; Z.Z. and L.-M.P. designed the experiment; C.Q. and Y.Y. performed the device fabrication and characterization; C.Q., M.X., and D.Z. grew the nanotubes; and Z.Z., C.Q., and L.-M.P. analyzed the data and co-wrote the manuscript. All the authors discussed the results and commented on the manuscript.

SUPPLEMENTARY MATERIALS

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6 September 2016; accepted 21 December 2016
10.1126/science.aaj1628

Editor's Summary

Moving transistors downscale

One option for extending the performance of complementary metal-oxide semiconductor (CMOS) devices based on silicon technology is to use semiconducting carbon nanotubes as the gates. Qiu *et al.* fabricated top-gated carbon nanotube field-effect transistors with a gate length of 5 nm. Thin graphene contacts helped maintain electrostatic control. A scaling trend study revealed that, compared with silicon CMOS devices, the nanotube-based devices operated much faster and at much lower supply voltage, and they approached the limit of one electron per switching operation.

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