Field Programmable Gate Array

FPGA

Laboratorio de electrónica

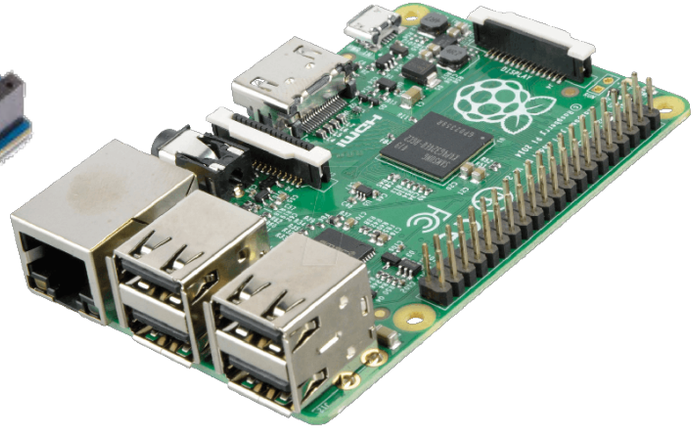
Dispositivos embebidos

"Era de la información"

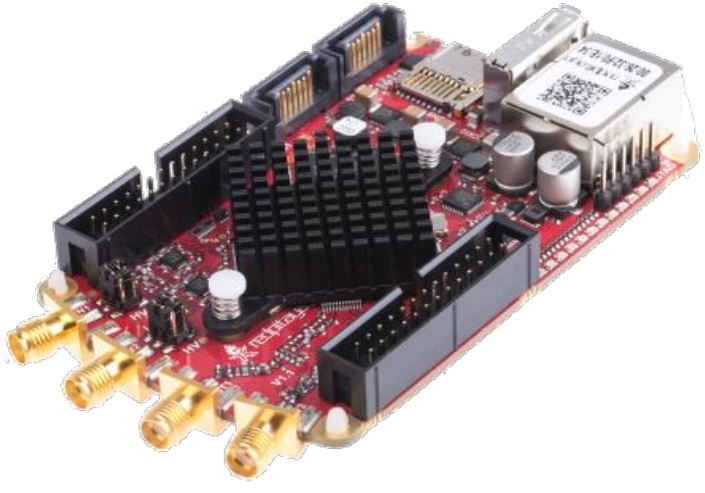
Embebidos:
computadora
+
electrónica específica

Arduino

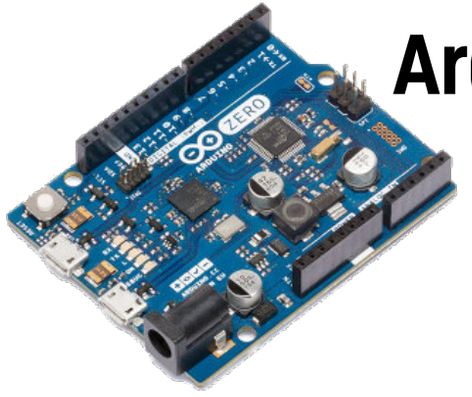
Raspberry Pi



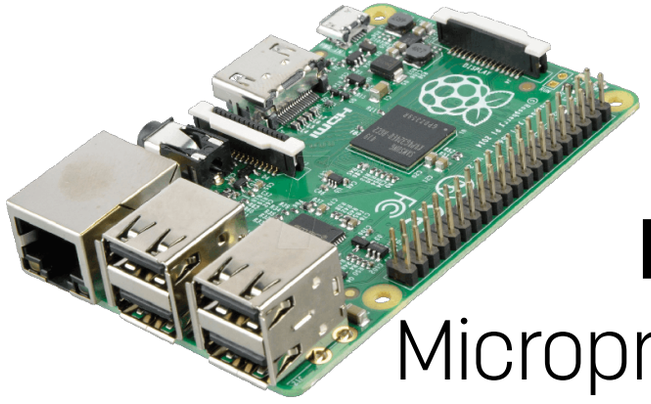
Red Pitaya



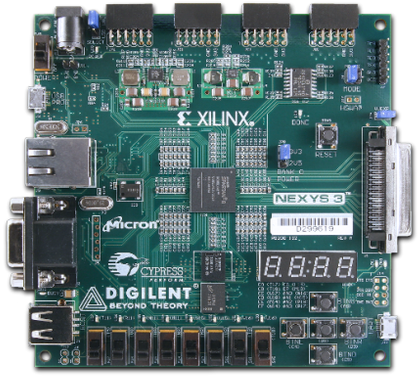
Embebidos programables



Arduino
Microcontrolador

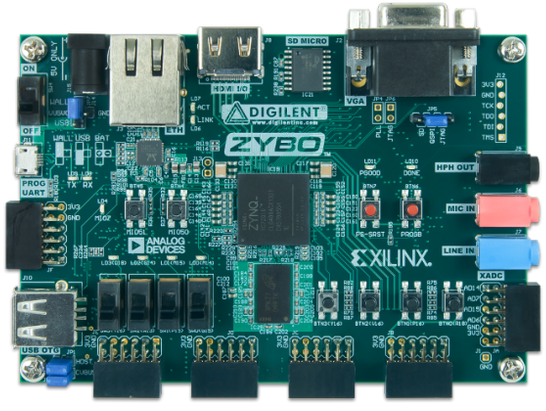


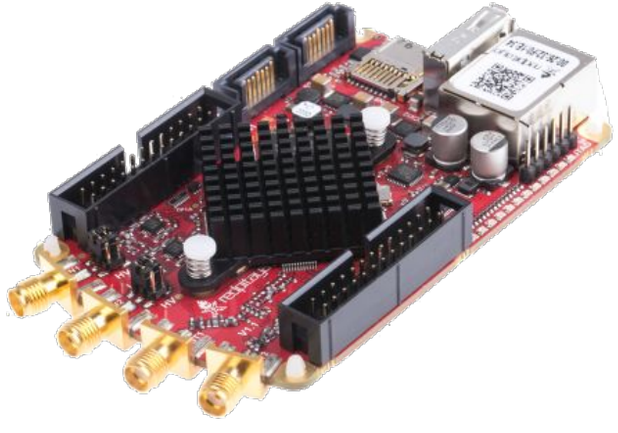
Raspberry
Microprocesador



Nexys3
FPGA "pura"

Zybo
Micro+FPGA

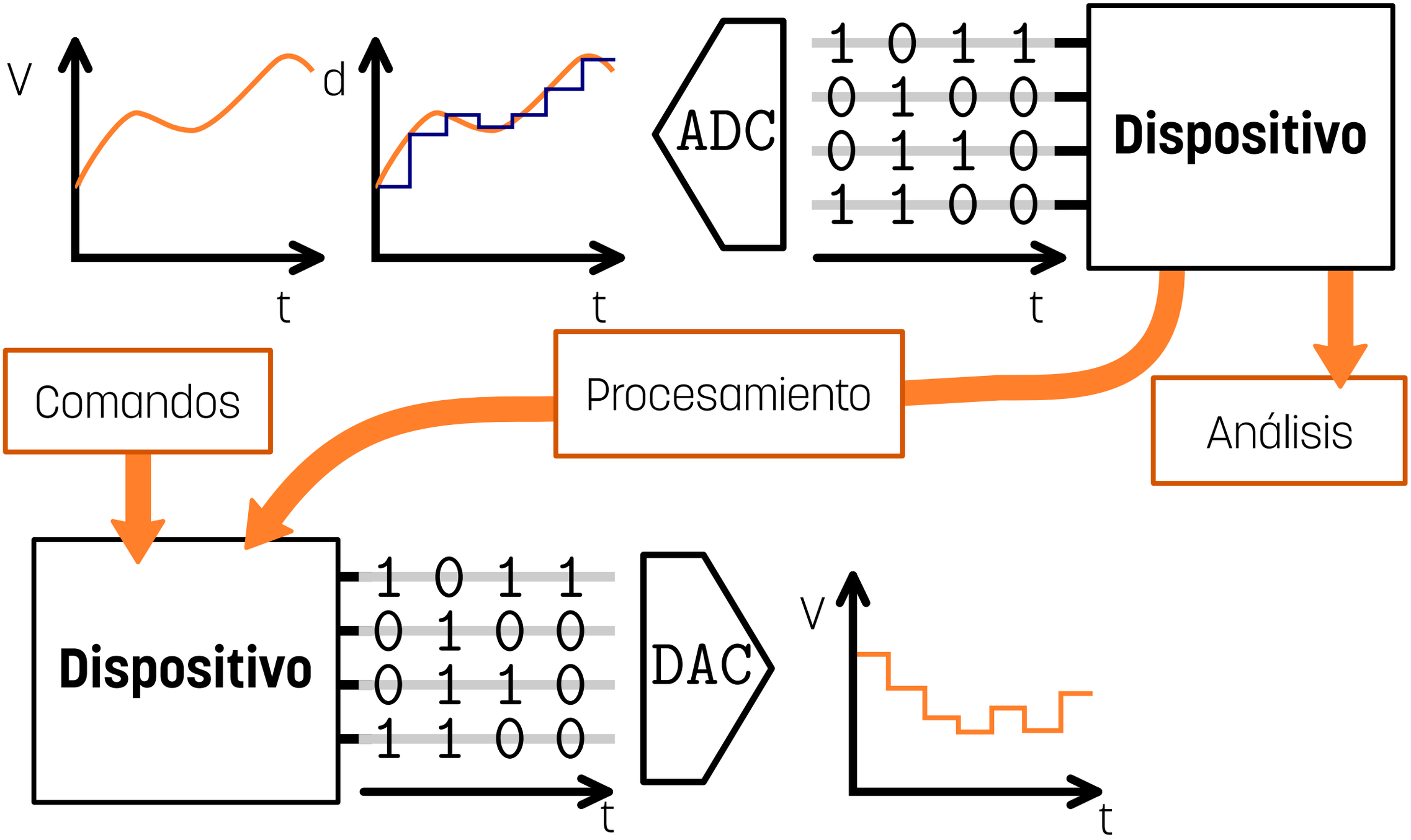




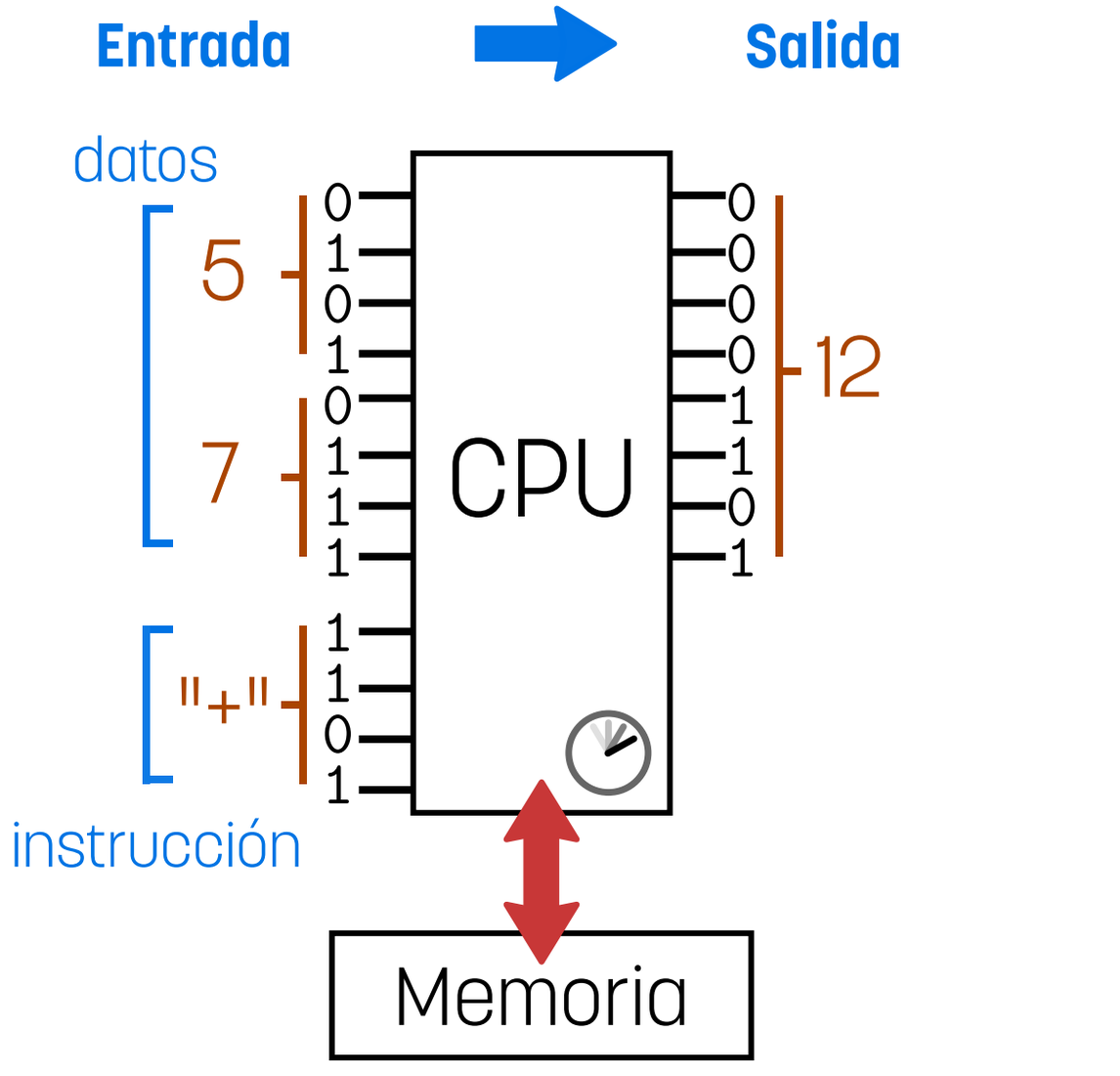
Red Pitaya
Micro+FPGA

Orientada a procesamiento analógico
Parte en software libre → Comunidad

Adquisición, control y procesamiento



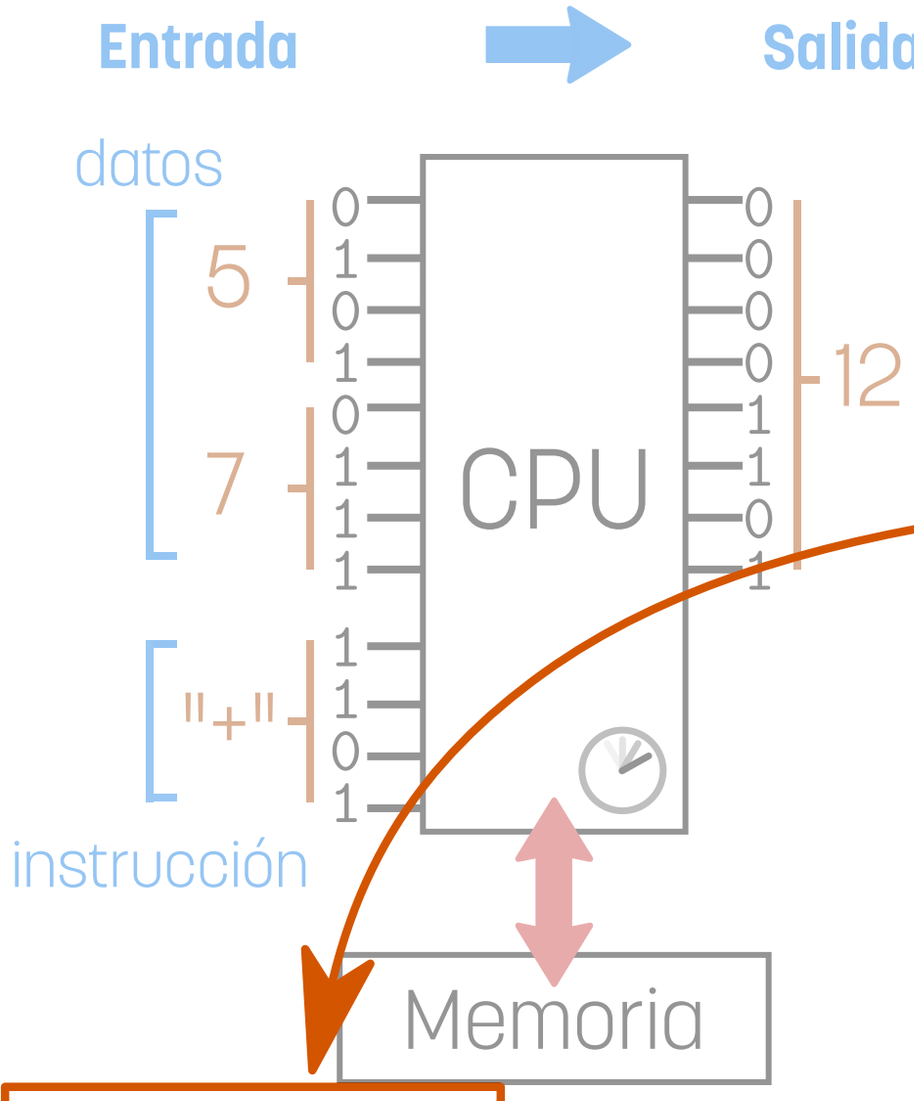
Micro vs FPGA



MOV, PUCH, CALL,
CMP, ADD, POP ...

Microprocesador

Micro vs FPGA

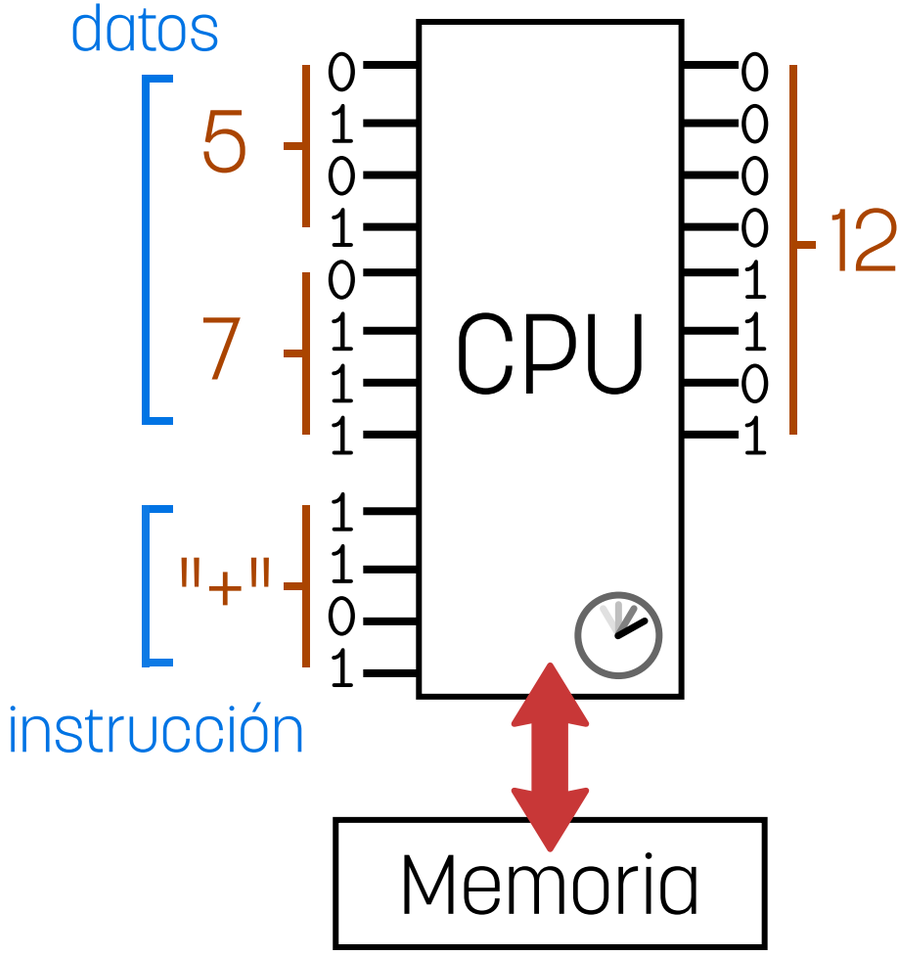



```c
#include <stdio.h>
int main()
{
      int i, j, rows;

      printf("Enter number of rows: ");
      scanf("%d",&rows);

      for(i=1; i<=rows; ++i)
      {
            for(j=1; j<=i; ++j)
            {
                  printf("* ");
            }
            printf("\n");
      }
      return 0;
}
```

Algoritmo

Micro vs FPGA

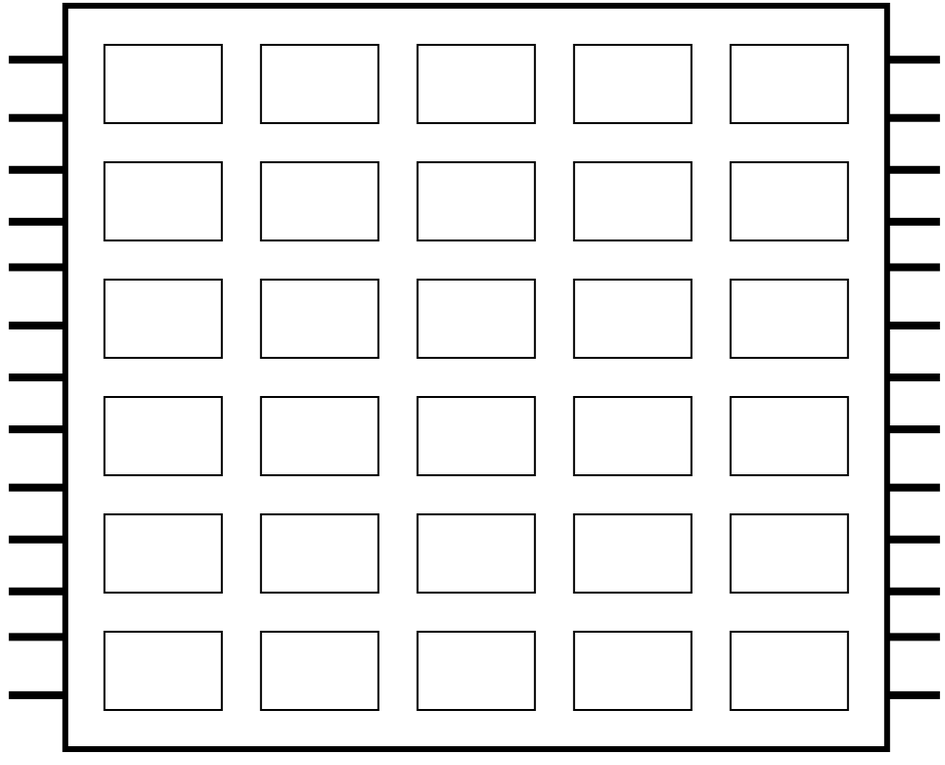
Entrada → **Salida**



MOV, PUCH, CALL,
CMP, ADD, POP ...

Microprocesador

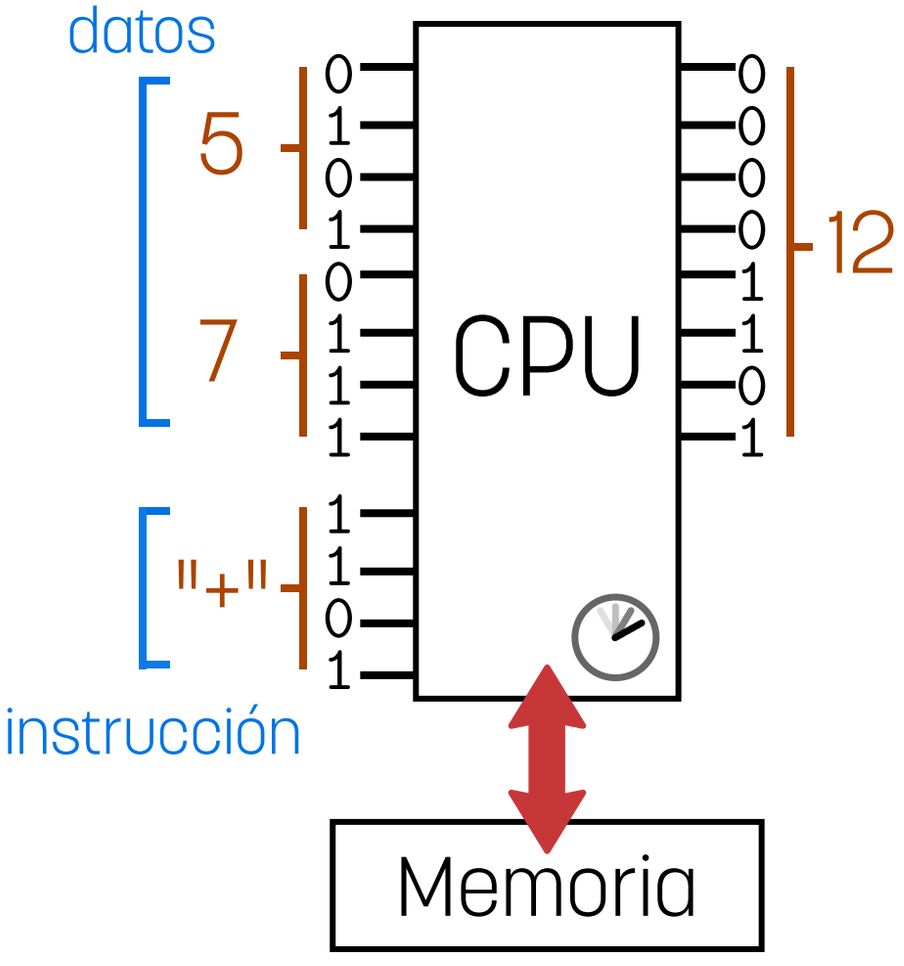
Entrada → **Salida**



FPGA

Micro vs FPGA

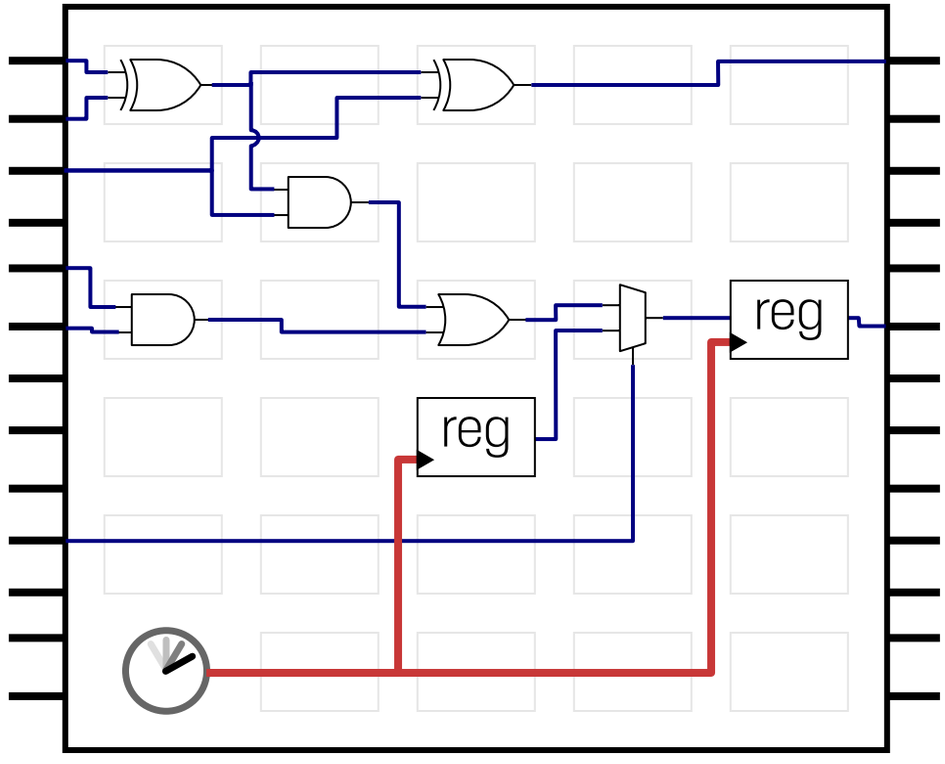
Entrada → **Salida**



MOV, PUCH, CALL,
CMP, ADD, POP ...

Microprocesador

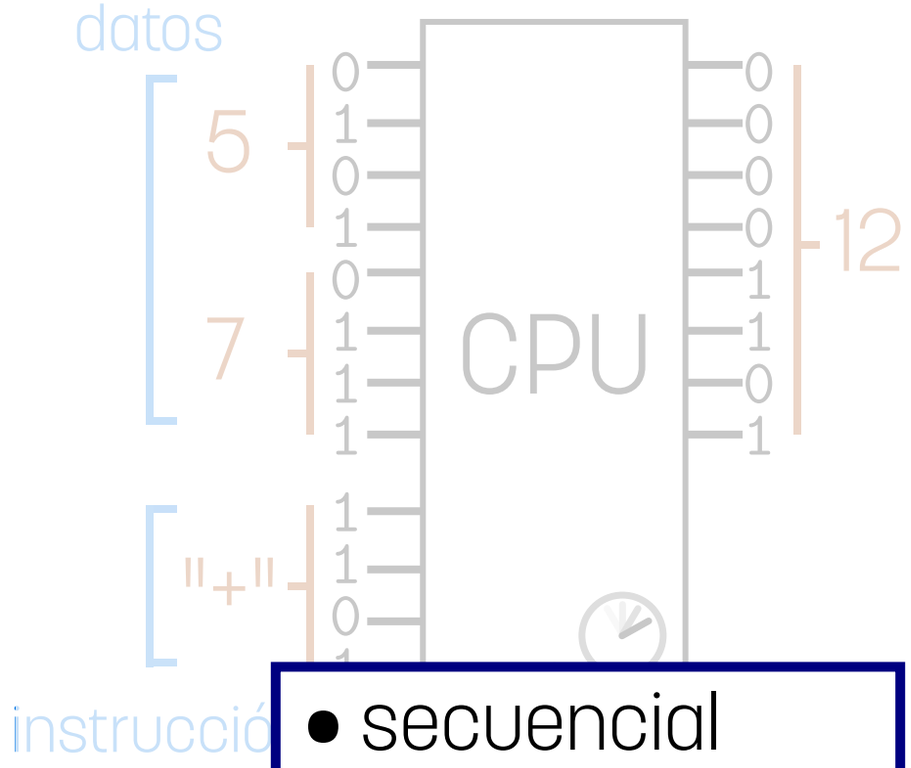
Entrada → **Salida**



FPGA

Micro vs FPGA

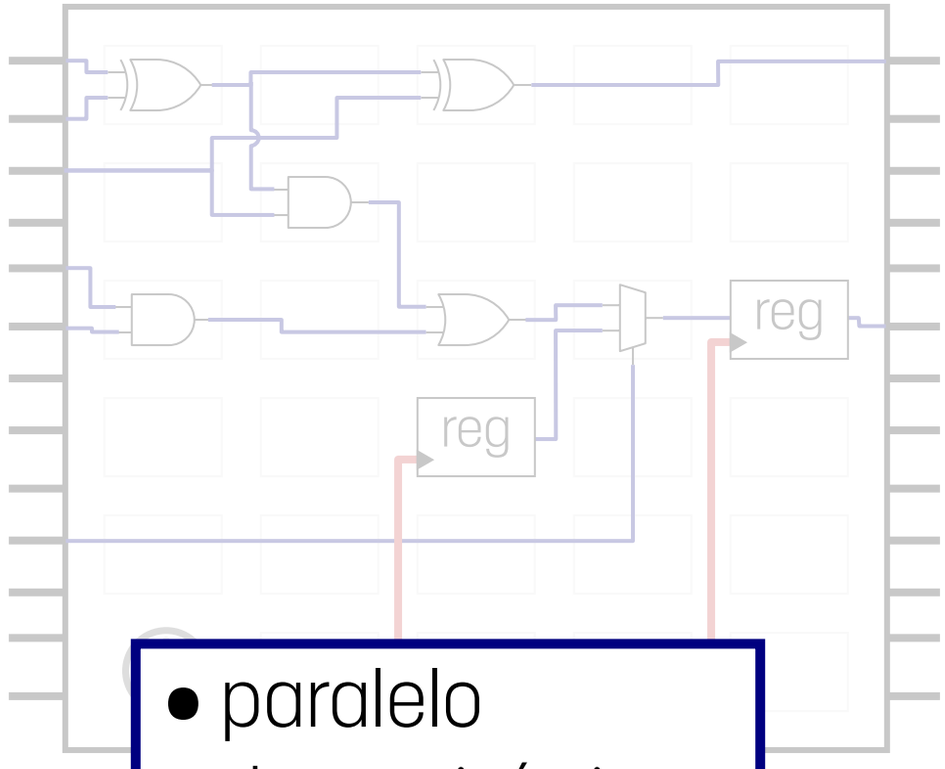
Entrada → Salida



- secuencial
- indeterminístico
- versátil

Microprocesador

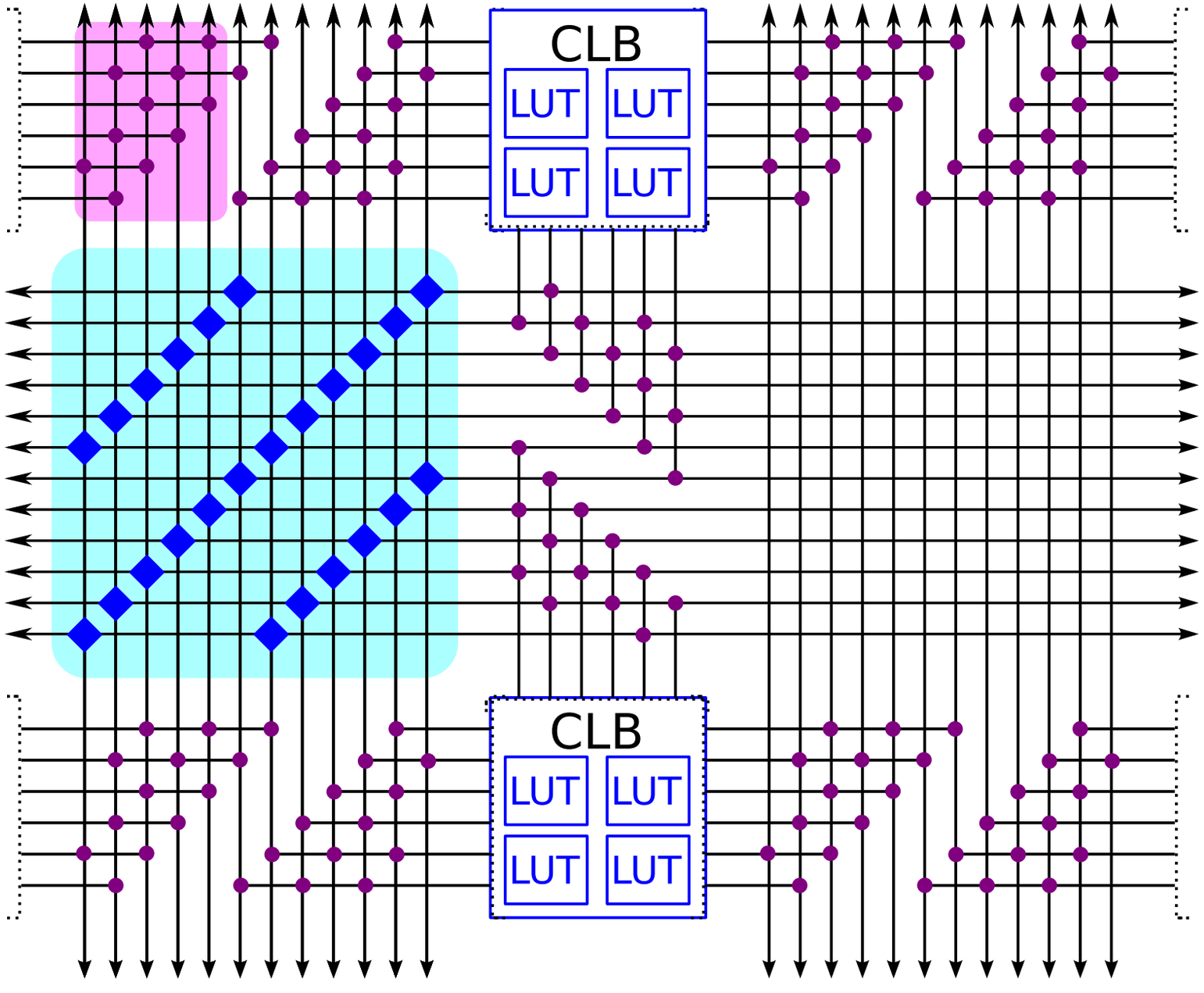
Entrada → Salida



- paralelo
- determinístico
- rígido

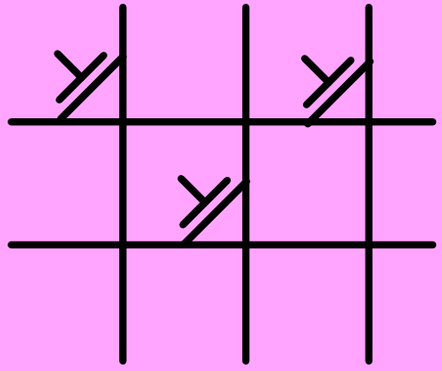
FPGA

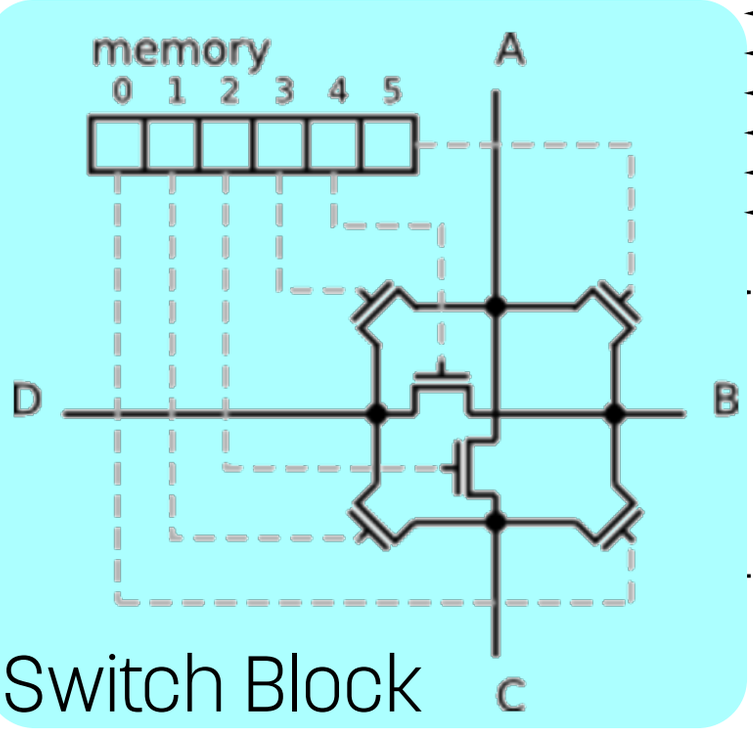
Enrutado



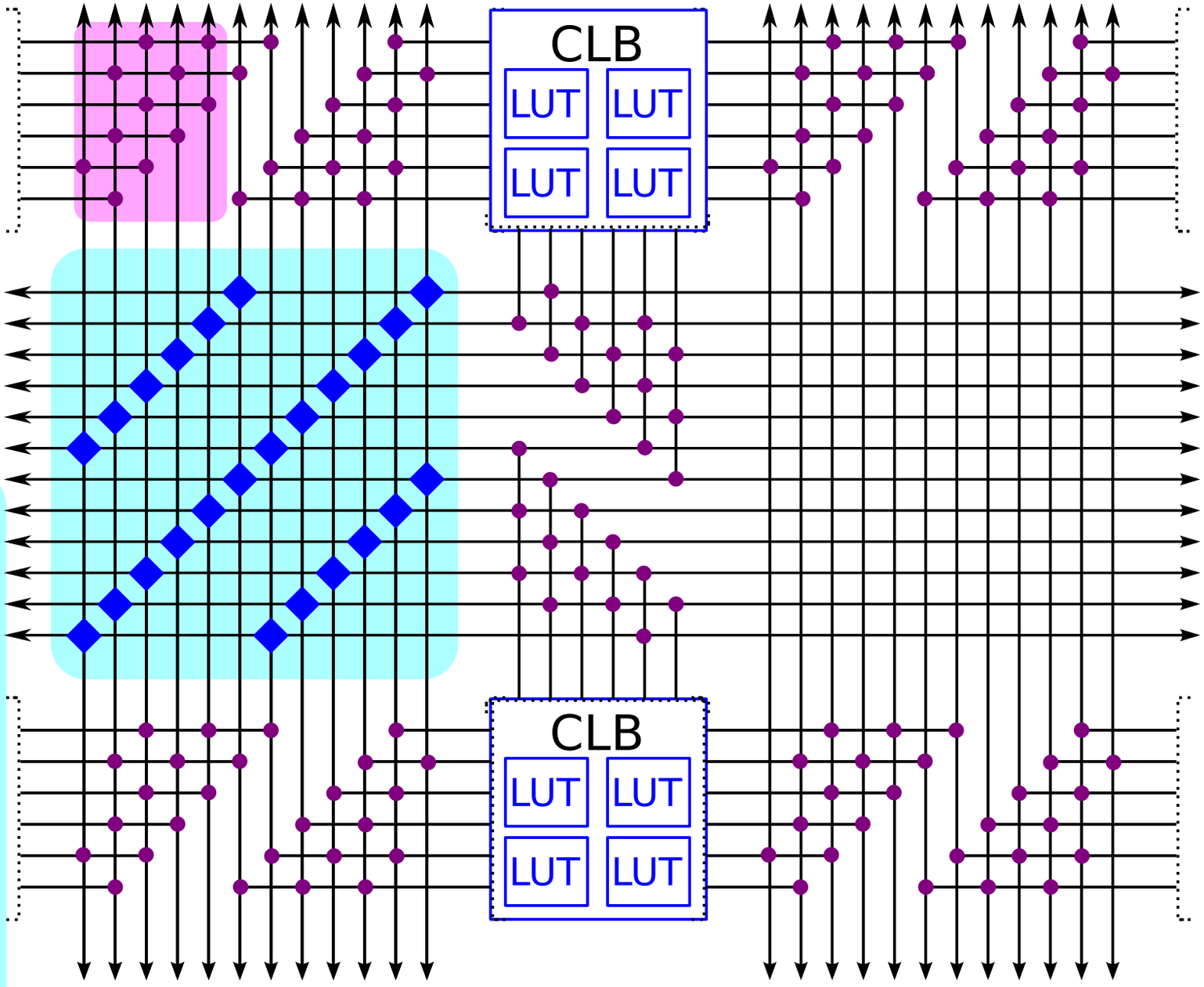
Enrutado

Conectión Block

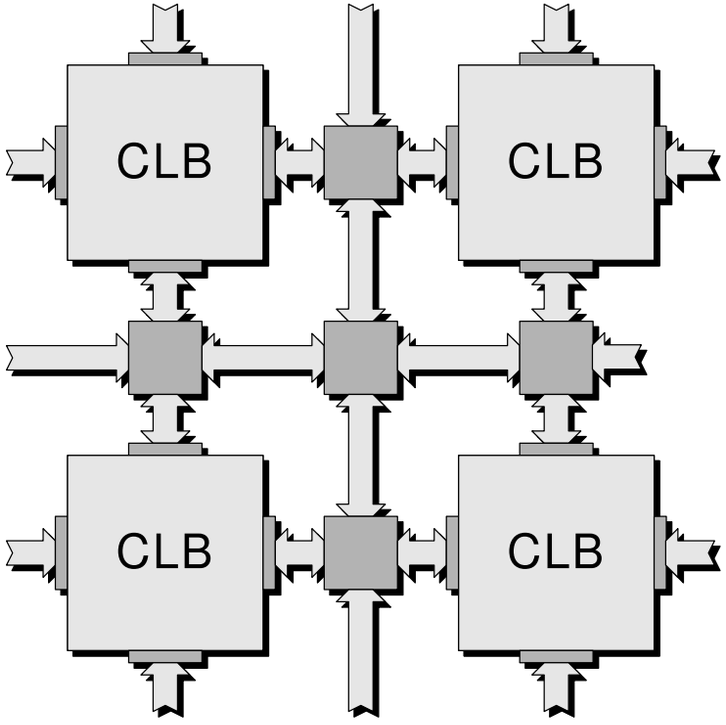




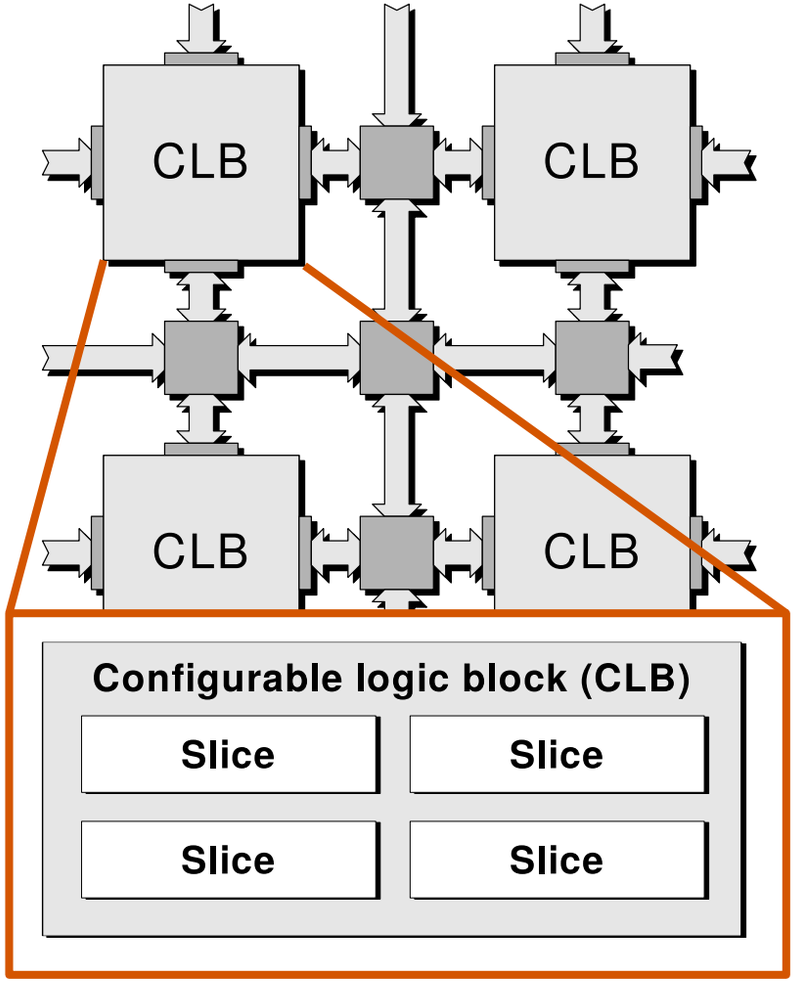
Switch Block



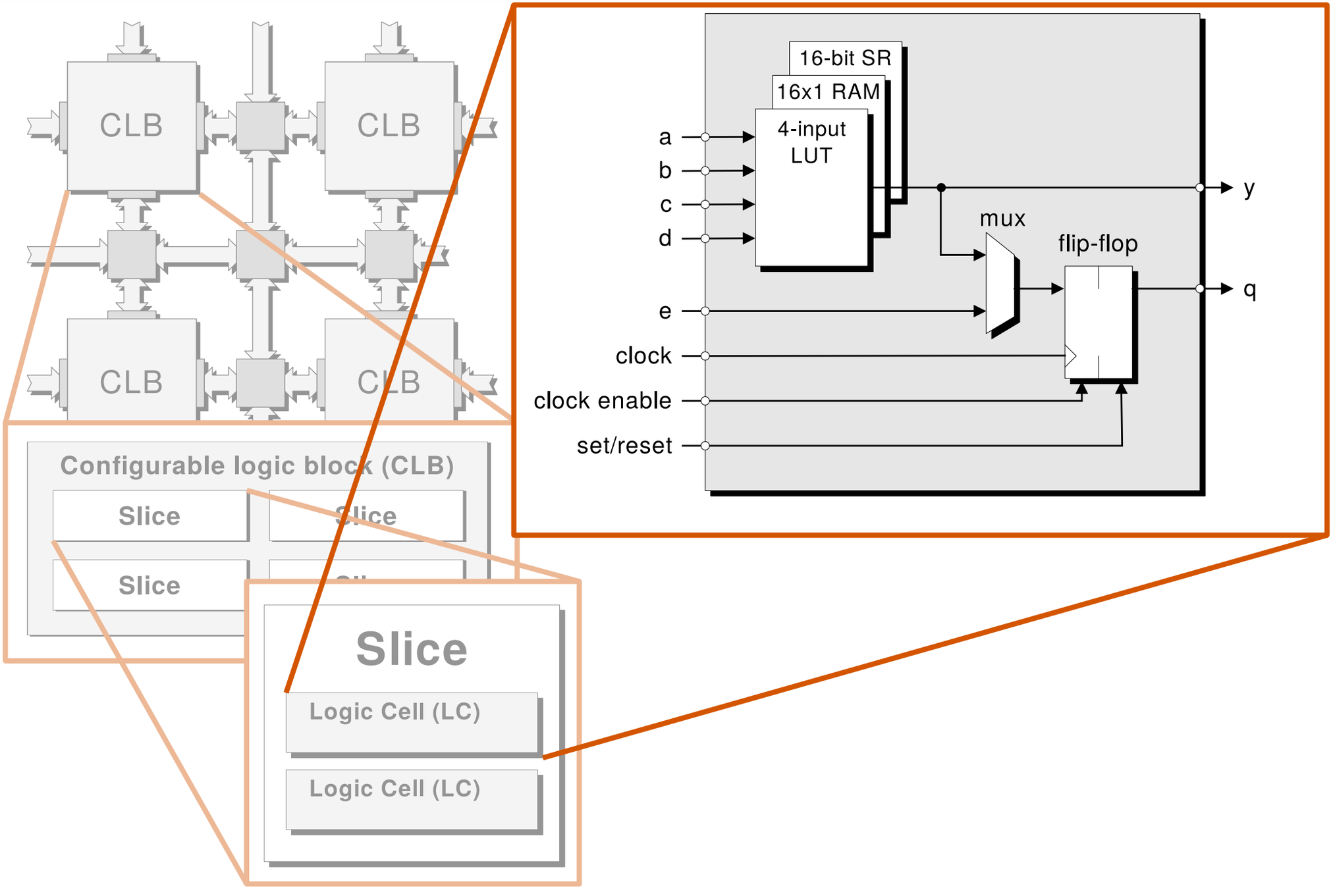
Estructura



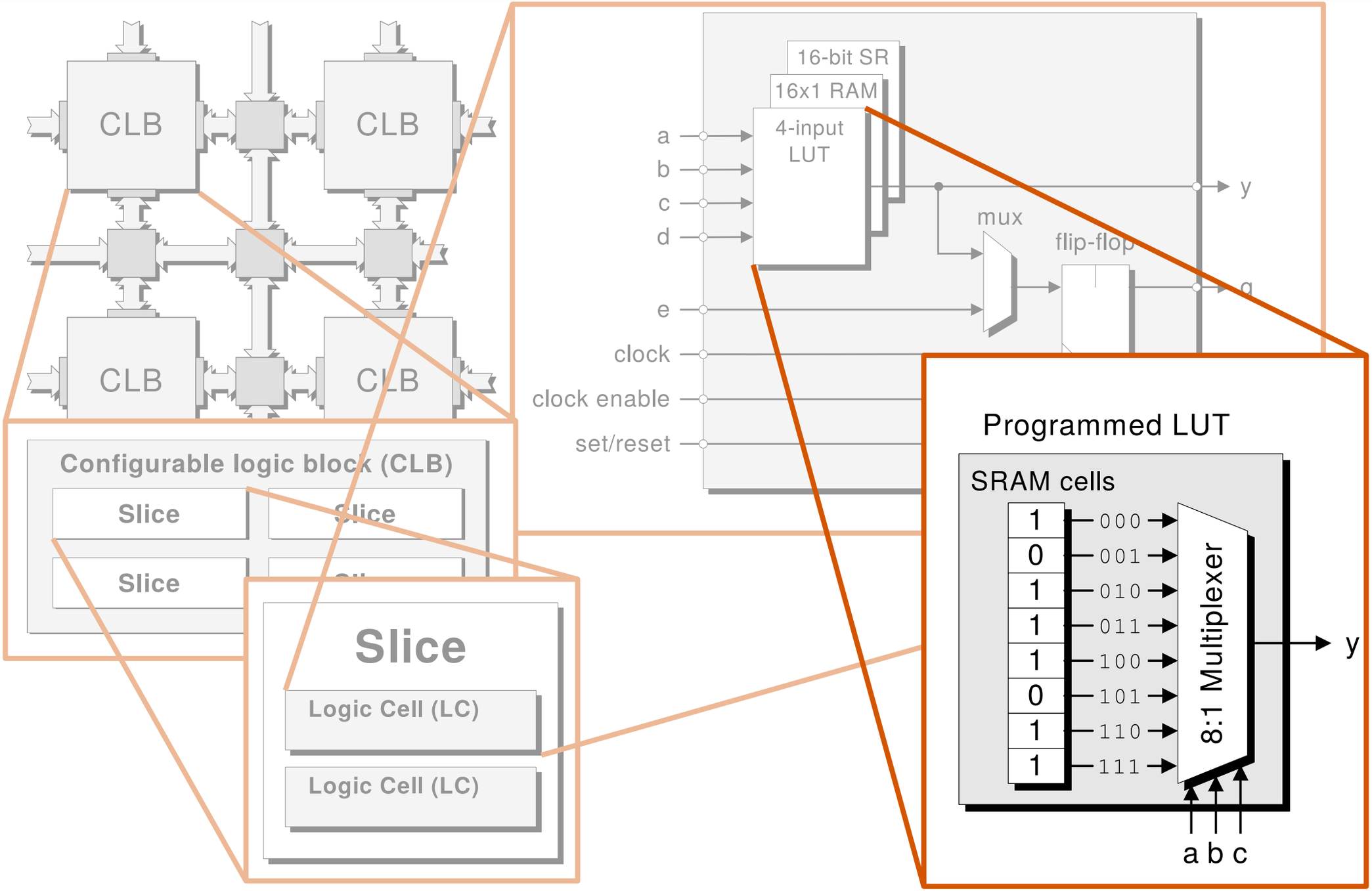
Estructura

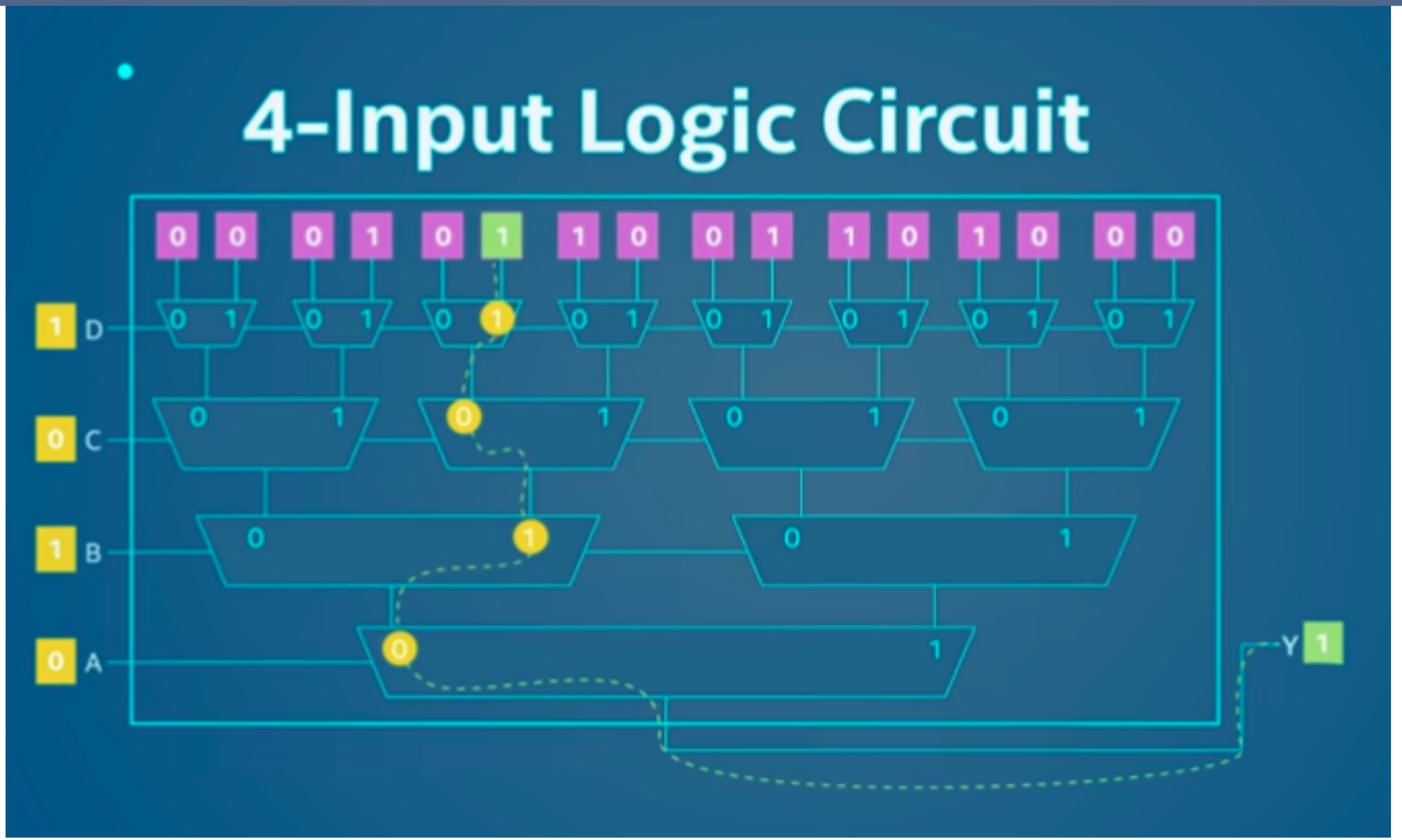

CLB
CLB
CLB
CLB
Configurable logic block (CLB)
Slice
Slice
Slice
Slice

Estructura

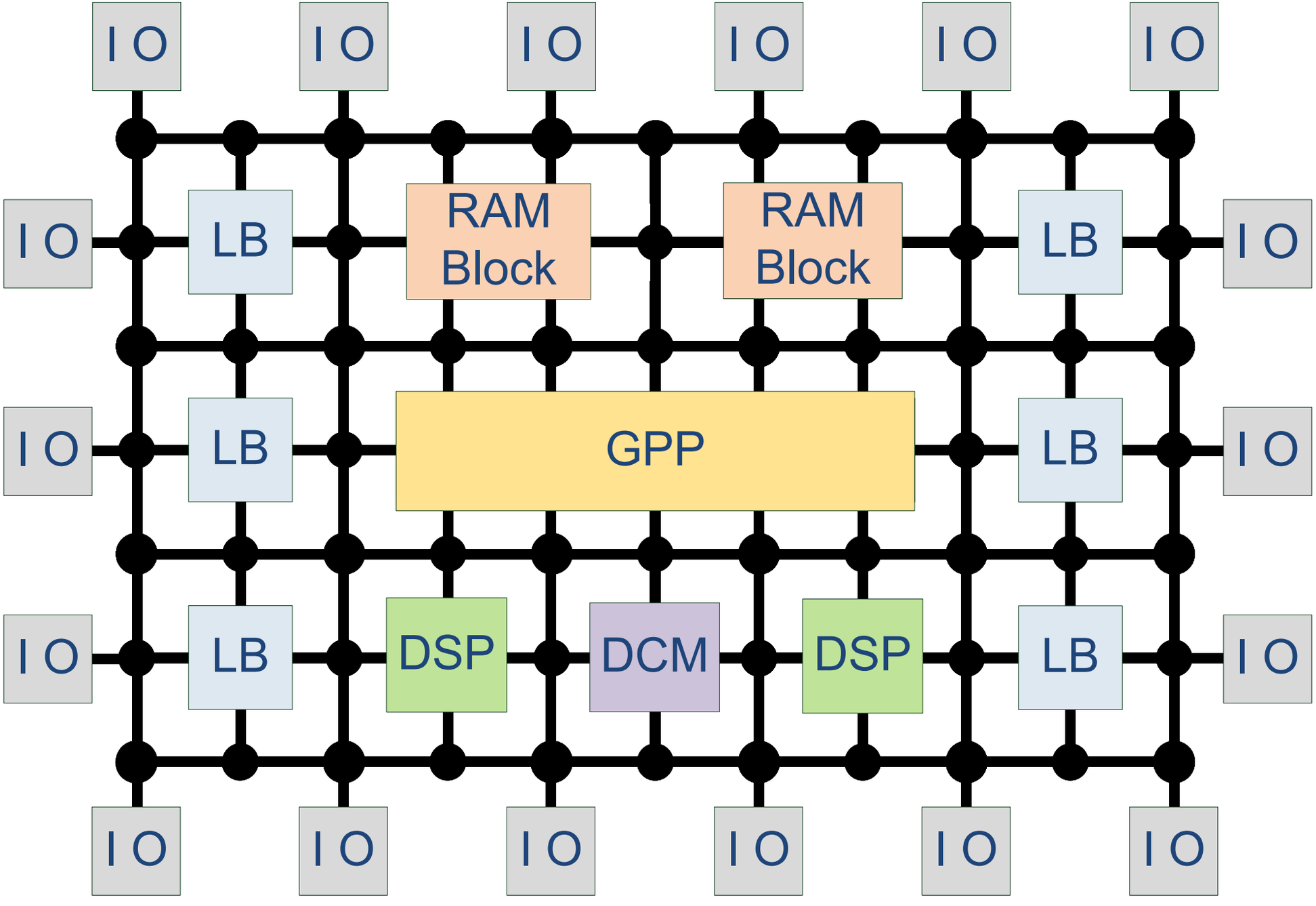

CLB
CLB
CLB
CLB
Configurable logic block (CLB)
Slice
Slice
Slice
Slice
Logic Cell (LC)
Logic Cell (LC)
16-bit SR
16x1 RAM
4-input
LUT
a
b
c
d
e
clock
clock enable
set/reset
mux
flip-flop
y
q

Estructura


CLB
CLB
CLB
CLB
Configurable logic block (CLB)
Slice
Slice
Slice
Slice
Logic Cell (LC)
Logic Cell (LC)
16-bit SR
16x1 RAM
4-input LUT
a
b
c
d
e
clock
clock enable
set/reset
mux
flip-flop
y
q
Programmed LUT
SRAM cells
1
0
1
1
1
0
1
1
000
001
010
011
100
101
110
111
8:1 Multiplexer
y
a b c


4-Input Logic Circuit
0 0 0 1 0 1 1 0 0 1 1 0 1 0 0 0
1 D
0 C
1 B
0 A
Y 1

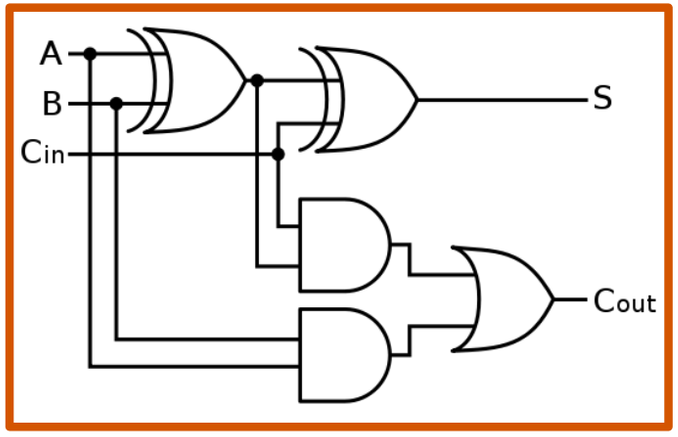
Estructura


I O
I O
I O
I O
I O
I O
I O
LB
RAM Block
RAM Block
LB
I O
I O
LB
GPP
LB
I O
I O
LB
DSP
DCM
DSP
LB
I O
I O
I O
I O
I O
I O
I O

Diseño RTL

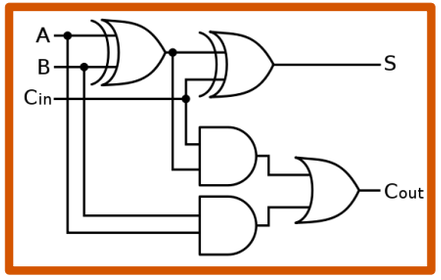
Código a lógica combinacional

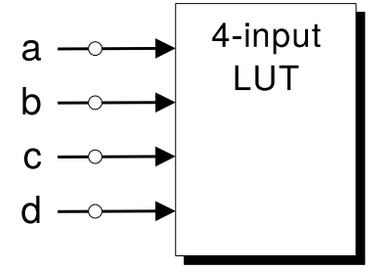
```
module  mux_using_assign(
din_0       , // Mux first input
din_1       , // Mux Second input
sel         , // Select input
mux_out       // Mux output
);
//-----------Input Ports---------------
input din_0, din_1, sel ;
//-----------Output Ports---------------
output mux_out;
//------------Internal Variables--------
wire  mux_out;
//-------------Code Start-----------------
assign mux_out = (sel) ? din_1 : din_0;

endmodule //End Of Module mux
```



Síntesis

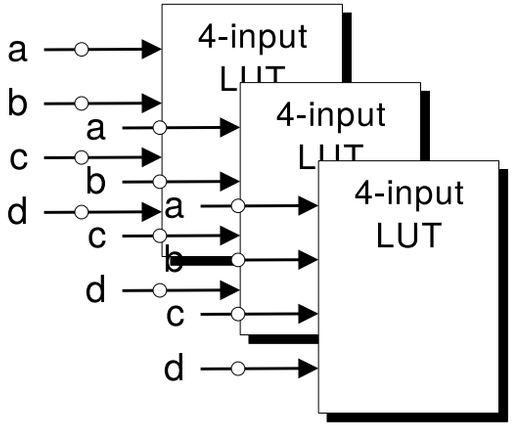
Lógica combinacional a combinación de LUTS

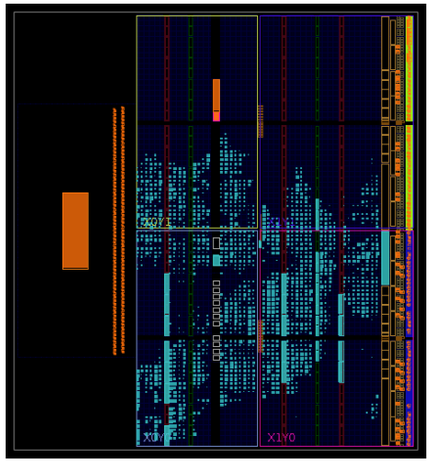




Implementación

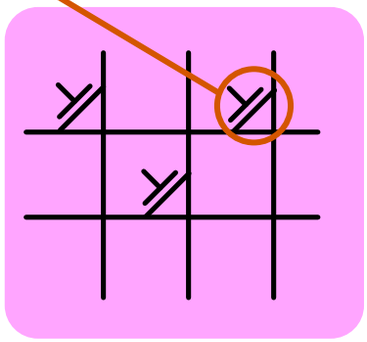
Cableado según el hardware disponible

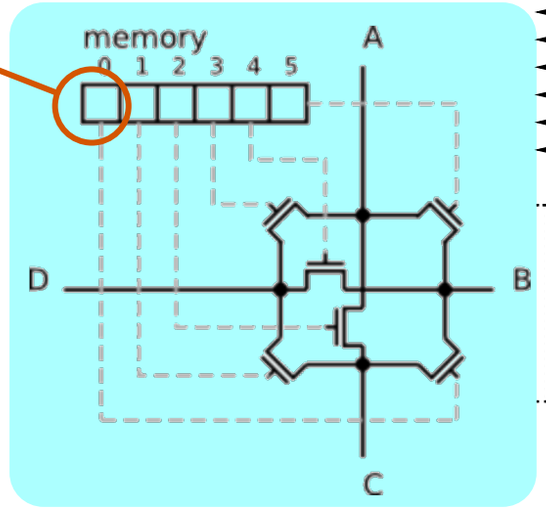


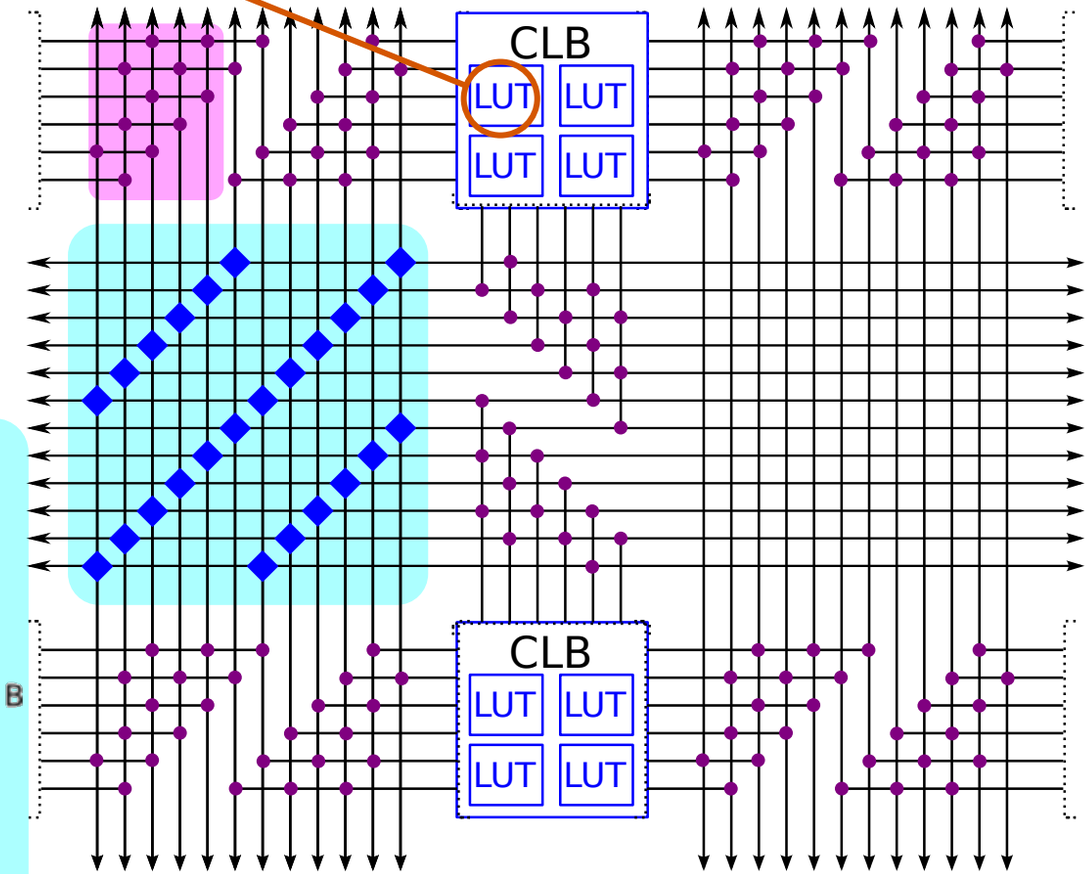


Implementación

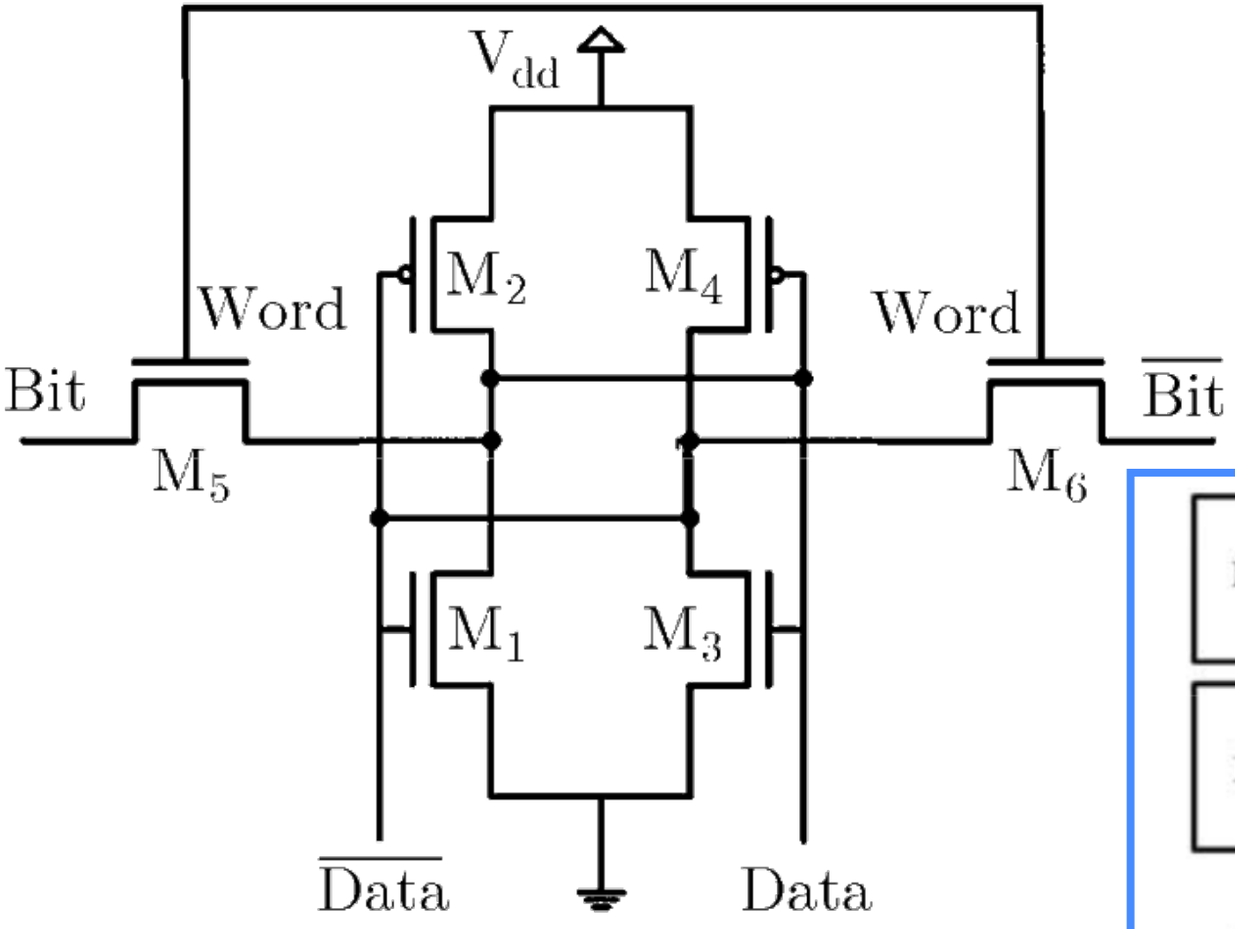

```
1101100010010
1111100011010
0100111100110
0001000110001
0100110100010
0110100111010
1010001010100
0010000000001
0101000111001
```





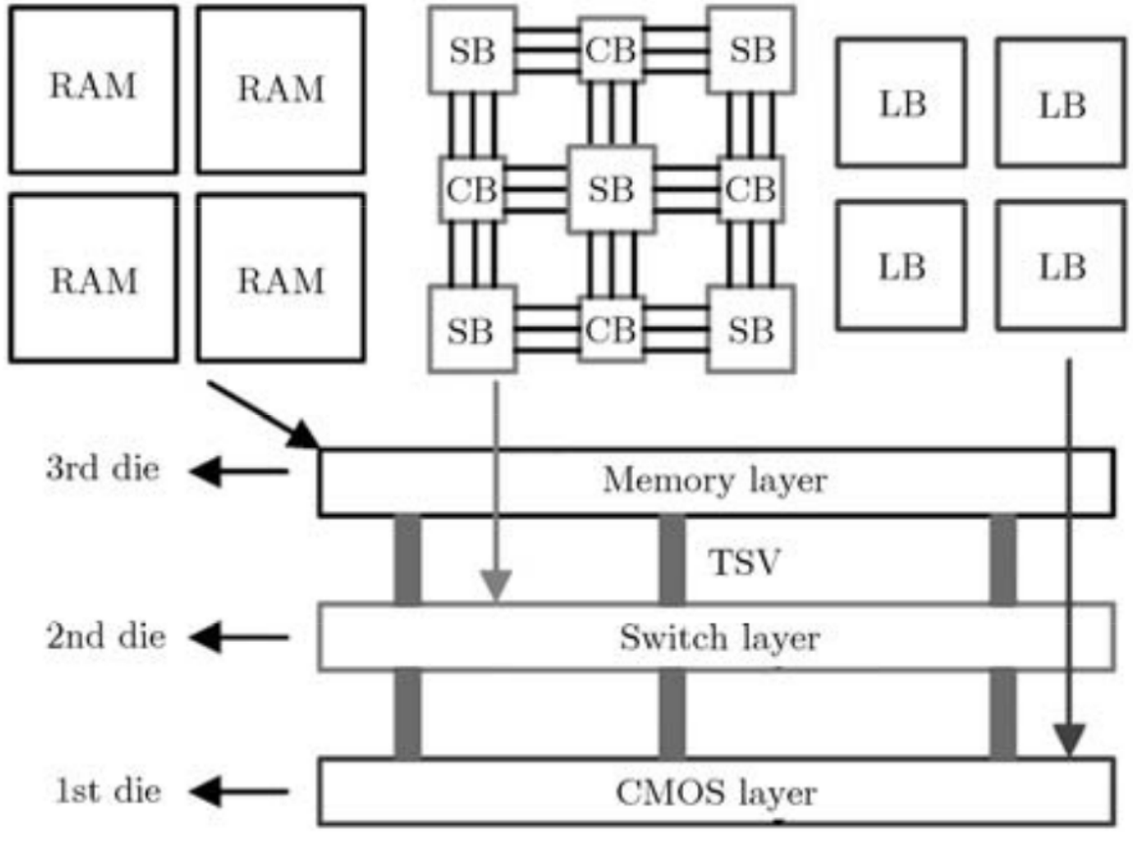


Memoria SRAM y capas del integrado

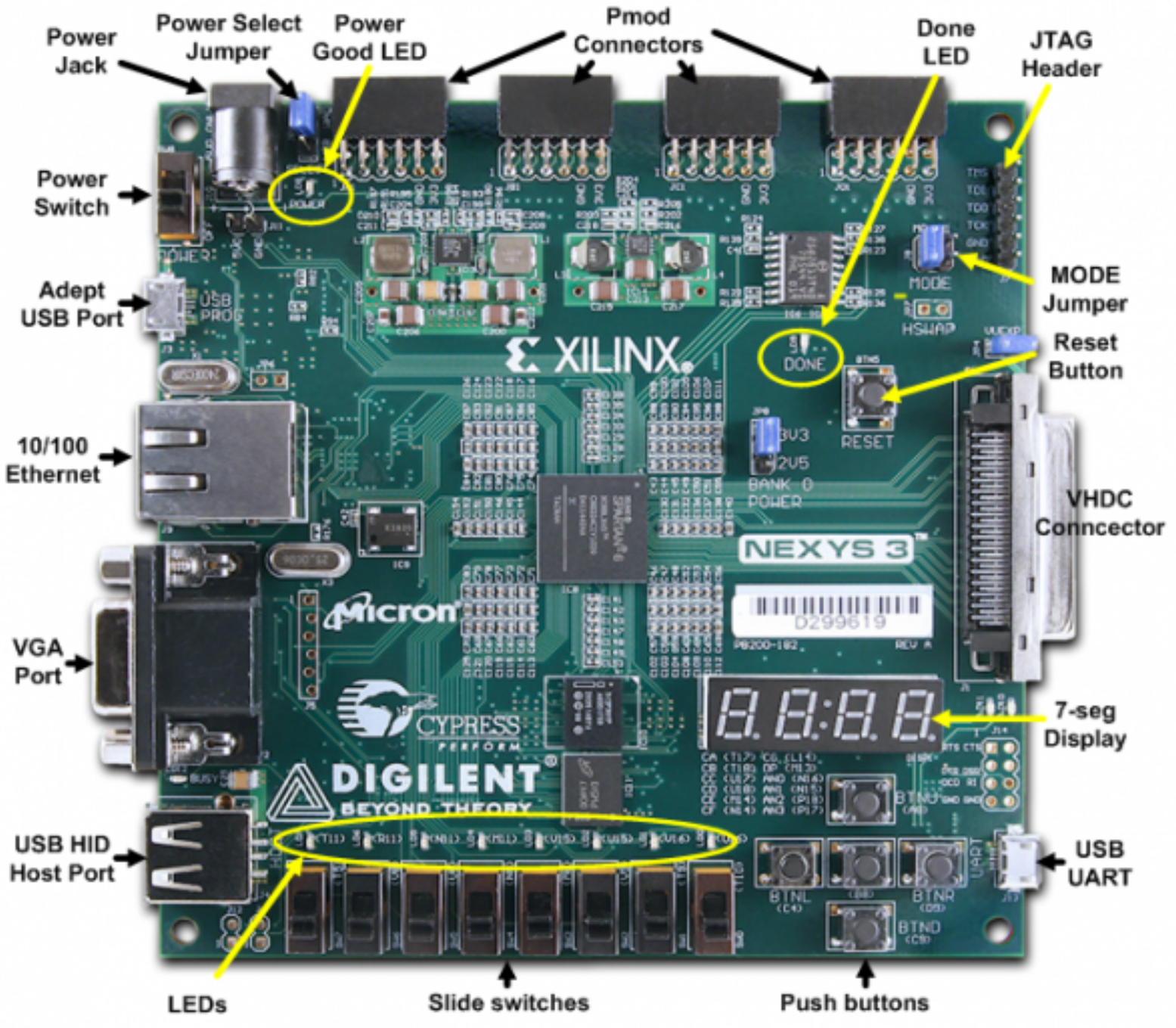


SRAM

Capas



Periféricos



Micro + FPGA

Extensión analógica
~100 kS/s, ~12 bits, 0-1.8 V
4 ADC AS, 4 DAC PWM

DDR3 RAM
512 MB

microSD
Unidad SO y diseño FPGA

micro USB
Alimentación 5 V, 2 A

Entrada analógica rápida
125 MS/s, 14 bits, ±1 V

micro USB
consola SO

Salida analógica rápida
125 MS/s, 14 bits, ±1 V

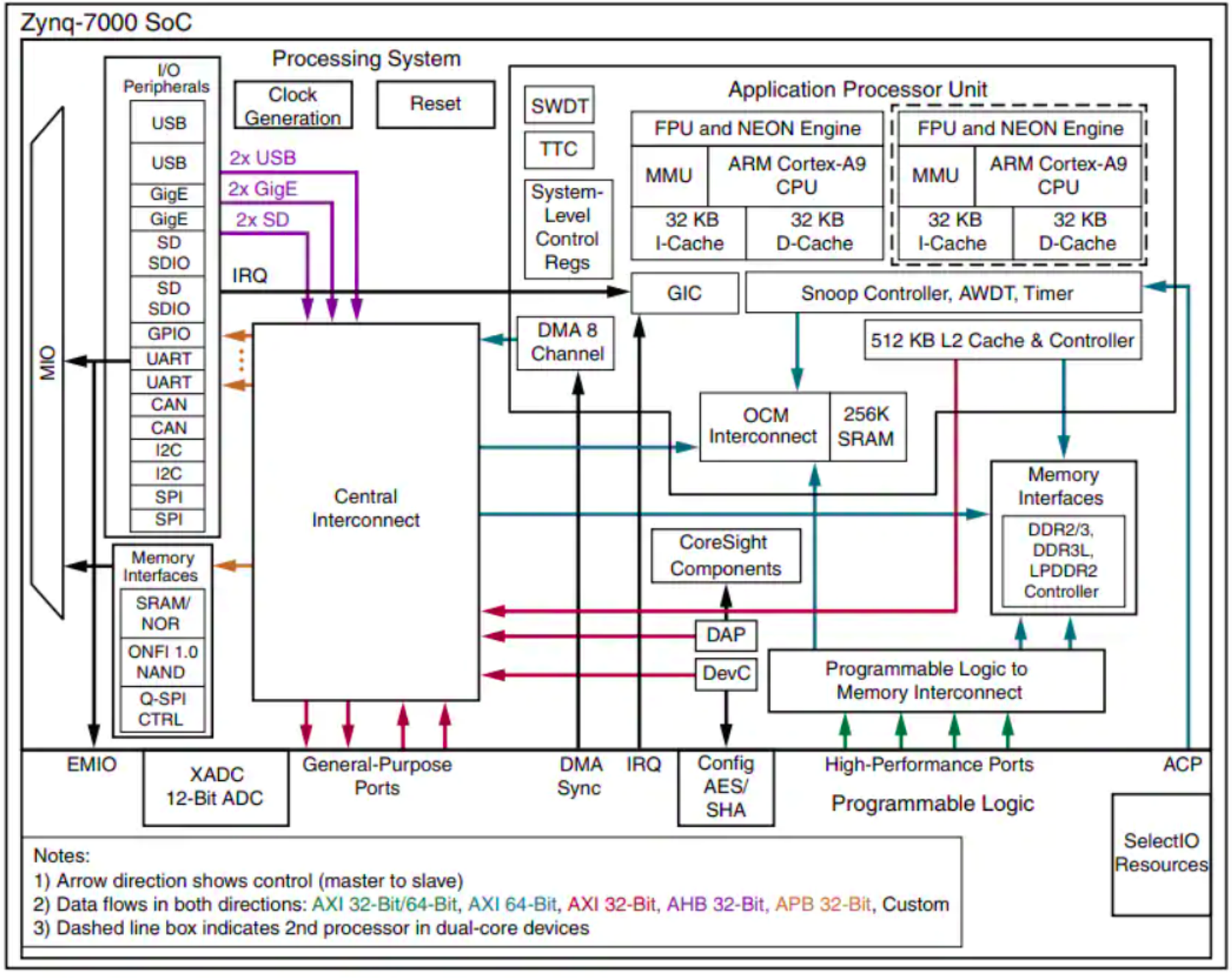
USB

Ethernet
1 Gb/s

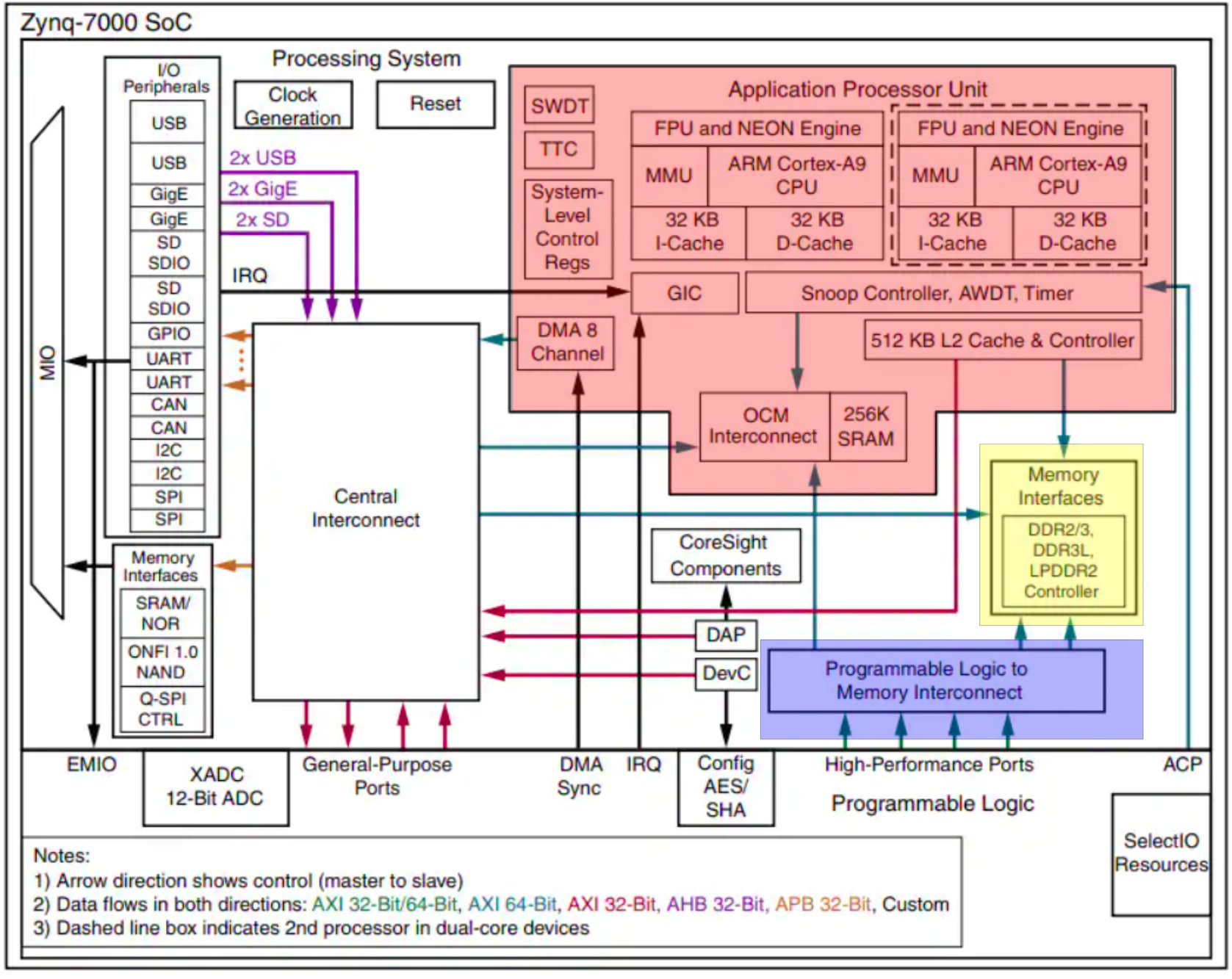
Extensión digital
16 E/S, 125 MS/s, 3.3 V

Microprocesador + FPGA
Dual core ARM-Cortex A9 Zync SoC

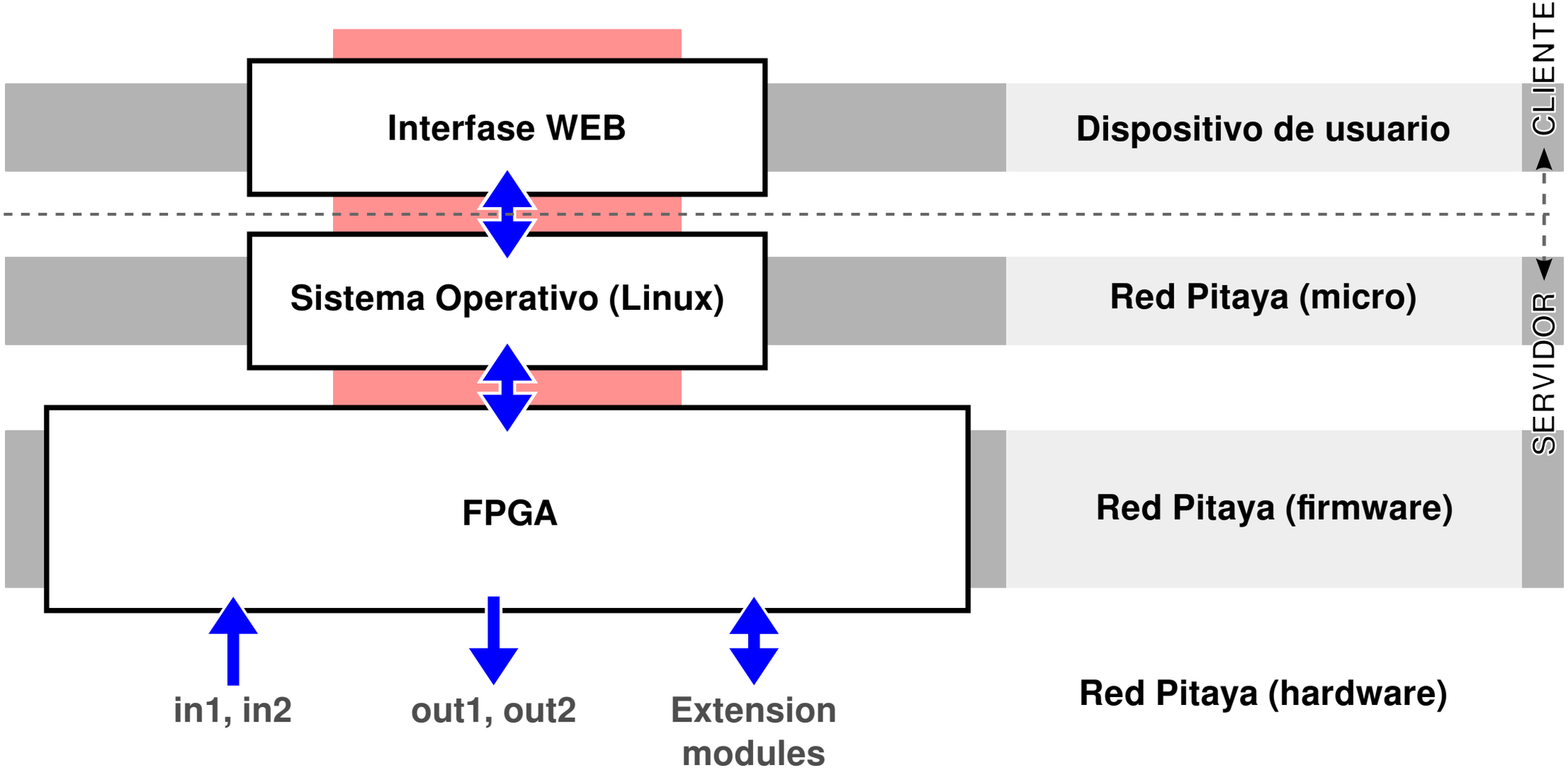
System on Chip (SoC)



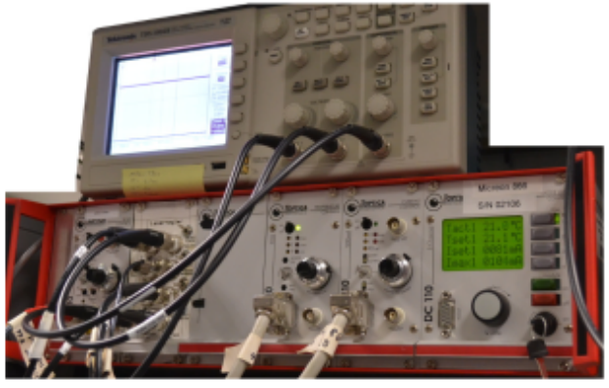
System on Chip (SoC)



System on Chip (SoC)



Modulación + demodulación lock-in + PID



Osciloscopio

+

Filtros PID

Generador de funciones

Amplificador Lock-in

Diseño de instrumentos a medida para el laboratorio

Aplicaciones

- **Desarrollo de hardware**
  - Filtros
  - Pre-Procesamiento
  - Estabilización
- **Procesamiento en tiempo real**
- **Control realimentado**
  - Robótica
  - Impresoras 3D
  - Control fabril
- **Desarrollo de instrumentos a medida**
  - Osciloscopio
  - Lock-in
  - Generador de funciones
  - Generador de pulsos
  - DAQ
  - Frecuencímetro
- **Tareas específicas**
  - Criptografía
  - Minado de criptomonedas
- **Investigación**
  - Simulación de sistemas dinámicos
  - Simulación de evolución

- CERN
- LIAF
- Óptica cuántica
- Metrología
- Nuclear

Empresas, lenguajes

Empresas:

- Xilinx/AMD
- Altera
- Lattice
- Actel/Microsemi

Lenguajes:

- VHDL
- Verilog
- System-Verilog